

A product of the Chyron Group

TECHNICAL MANUAL

*September, 1986
Pub. No. 2A00769
Rev. 0 Change 0*

*© Copyright 1988
Chyron Corporation
All Rights Reserved*



*A member of The Chyron Group
The company the whole world watches*

Chyron Corporation • 265 Spagnoli Road • Melville, NY 11747 • (516) 845-2000

Table of Contents

<u>Section/ Para.</u>	<u>Title</u>	<u>Page</u>
1	INTRODUCTION	1-1
1.1	General	1-1
1.2	Approach	1-1
1.3	Content	1-2
2	ARCHITECTURAL OVERVIEW	2-1
2.1	System Introduction	2-1
2.1.1	Dual Processor P. C. Board	2-1
2.1.1.1	8088 Microprocessor	2-1
2.1.1.2	80186 Microprocessor	2-2
2.1.2	Font Memory P. C. Board	2-2
2.1.3	Main Logic P. C. Board	2-2
2.1.3.1	Memory	2-2
2.1.3.2	Color Generation	2-2
2.1.3.3	Video Address Generation	2-5
2.1.3.4	Video Controller	2-5
2.1.4	I/O P. C. Board	2-5
2.1.4.1	Keyboard Interface	2-5
2.1.4.2	Alarm Interface	2-5
2.1.4.3	Floppy-Disk Controller	2-5
2.1.4.4	Edit Channel	2-6
2.1.5	Sync Gen/Encoder P. C. Board	2-6
2.1.5.1	Digital Encoder	2-6
2.1.5.2	Video Mixer	2-6
2.1.5.3	Keyer Control	2-6
2.1.5.4	Genlocking Timing Generator	2-6
2.1.6	Power Supply	2-6
2.2	Image Generation	2-7
2.2.1	Run Length Encoding	2-7
2.2.1.1	Transition Code	2-7
2.2.1.2	Continuation Code	2-8
2.2.1.3	End-of-Scan/End-of-Field Codes	2-8
2.2.2	Frame Buffer	2-8
2.3	Video Generation	2-9
3	VP-2 FUNCTIONAL THEORY OF OPERATION	3-1
3.1	Dual-Processor Board	3-1
3.1.1	80816 CPU	3-1
3.1.2	8088 CPU	3-1
3.2	Font Memory P. C. Board	3-2
3.3	Main Logic P. C. Board	3-4
3.3.1	Address and Data Buses	3-4
3.3.2	Chip Select/Enable Logic	3-4
3.3.3	Memory Systems	3-4
3.3.4	Color Generation	3-8
3.3.5	Video Address Generation	3-8

Table of Contents (Continued)

<u>Section/ Para.</u>	<u>Title</u>	<u>Page</u>
3.3.6	Video Controller	3-8
3.3.7	Key Controller	3-8
3.4	I/O Board Functional Description	3-9
3.4.1	Decoding Logic	3-11
3.4.2	Keyboard Interface	3-11
3.4.3	Alarm Interface	3-12
3.4.4	Edit Channel/Video Display Processor	3-12
3.4.5	Floppy Disk Controller	3-15
3.5	Sync Gen/Encoder P. C. Board	3-17
3.5.1	Digital Encoder	3-17
3.5.2	Video Mixer	3-18
3.5.3	Keyer Control	3-18
3.5.4	Genlocking Timing Generator	3-21
4	TROUBLESHOOTING	4-1
4.1	Introduction	4-1
4.2	Quick Troubleshooting Guide	4-2
4.3	Power Supply Diagnosis Procedure	4-4
4.4	Dual Processor P. C. Board Diagnostic Procedure	4-6
4.4.1	Initial Troubleshooting	4-6
4.4.1.1	80186 CPU Removal/Re-Seating	4-7
4.4.2	Troubleshooting from Run-Light Situations	4-8
4.4.2.1	8088 Run-Light On, 80186 Run-Light Off	4-8
4.4.2.2	8088 Run-Light Off, 80186 Run-Light Off	4-11
4.4.3	General CPU Troubleshooting Hints	4-12
4.4.3.1	80186 CPU Address/Data Line Troubleshooting	4-12
4.4.3.2	8088 CPU Address/Data Line Troubleshooting	4-12
4.4.4	Troubleshooting from Error Messages	4-13
4.5	Font Memory P. C. Board Troubleshooting	4-14
4.6	Main Logic P. C. Board Troubleshooting	4-15
4.6.1	Interrupt Controller Failures	4-15
4.6.2	CPU/Arbitration Clock Signal Troubleshooting	4-16
4.6.3	Troubleshooting from Error Messages	4-17
4.7	I/O P. C. Board Troubleshooting	4-18
4.7.1	Edit Channel Troubleshooting	4-18
4.7.2	Floppy Disk Controller Troubleshooting	4-21
4.7.3	Keyboard Interface Troubleshooting	4-23
4.7.4	Alarm Interface Troubleshooting	4-24
4.8	Sync Gen/Encoder P. C. Board Troubleshooting	4-25
4.8.1	Stand Alone B&W Verification	4-25
4.8.2	Stand Alone Color Verification	4-25
4.8.3	Genlocked B&W Verification	4-25
4.8.4	Genlocked Color Verification	4-26
4.8.5	Verification of Outputs to Main Logic Board	4-26
4.9	Board Removal Instructions	4-28
4.9.1	Initial Disassembly	4-28

Table of Contents (Continued)

<u>Section/ Para.</u>	<u>Title</u>	<u>Page</u>
4.9.2	Dual Processor Board Removal	4-29
4.9.3	Font Memory Board Removal	4-30
4.9.4	I/O Board Removal	4-31
4.9.5	Main Logic Board Removal	4-31
4.9.6	Sync Gen/Encoder Board Removal	4-32
4.9.7	Power Supply Removal	4-35
4.10	Shipping Instructions	4-35
4.10.1	General Packing Guidelines	4-35
4.10.2	General Shipping Instructions	4-35
5	VIDEO ALIGNMENT PROCEDURE	5-1
5.1	Introduction	5-1
5.2	Adjustment Procedure	5-2
5.2.1	Vertical Phase	5-2
5.2.2	Center Frequency	5-2
5.2.3	Subcarrier Frequency	5-3
5.2.4	Encoder Gain	5-3
5.2.5	V Axis Gain (Chroma Gain)	5-3
5.2.6	U Axis Gain	5-4
5.2.7	Program Gain	5-4
5.2.8	Program DC	5-4
5.2.9	Program HF	5-4
5.2.10	Insert Gain	5-4
5.2.11	Insert DC	5-4
5.2.12	Insert HF	5-4
5.3	User Adjustments Check	5-5
5.3.1	Horizontal Phase	5-5
5.3.2	Coarse Subcarrier Phase	5-5
5.3.3	Fine Subcarrier Phase	5-5
5.3.4	Key Mix Rate	5-5
5.3.5	Key Timing Adjust	5-5
6	PARTS LISTS	6-1
6.1	Introduction	6-1
6.2	Complete Assemblies	6-1
6.3	Dual Processor P. C. Board	6-2
6.4	Font Memory P. C. Board	6-3
6.5	Main Logic P. C. Board	6-4
6.6	I/O P. C. Board	6-8
6.7	Sync Generator/Encoder P. C. Board	6-11
6.8	Dual Oscillator P. C. Board	6-16
7	SCHEMATIC DIAGRAMS	7-1
7.1	Introduction	7-1
7.2	Contents	7-1

List of Illustrations

<u>Figure No.</u>	<u>Title</u>	<u>Page</u>
2-1	VP-2 Character Generator Functional Block Diagram	2-3
2-2	Transition Code Format	2-8
2-3	Continuation Code Format	2-8
3-1	Dual Processor P. C. Board Block Diagram	3-3A
3-2	Font Memory Board P. C. Board Block Diagram	3-3B
3-3	Main Logic P. C. Board Functional Block Diagram	3-5
3-4	VP-2 Memory Map	3-7
3-5	I/O Board Functional Block Diagram	3-10
3-6	Keyboard Interface Block Diagram	3-11
3-7	Alarm Interface	3-12
3-8	Edit Channel Block Diagram	3-14
3-9	FDC Block Diagram	3-16
3-10	Sync Gen/Encoder Block Diagram	3-19
4-1	Power Supply, Top View	4-4
4-2	80186 CPU Socket	4-6
4-3	80186 Assembly Drawing	4-7
4-4	Dual Processor Board Waveforms A, B, C, D	4-10
4-5	Interrupt Controller Jumpers	4-15
4-6	I/O Board Waveforms A, B, C	4-20
4-7	Sync Gen/Encoder Waveforms A, B	4-27
4-8	VP-2 Exploded View	4-33
5-1	Sync Gen/Encoder P. C. Board Adjustment Locations	5-7
7-1	Dual Processor P. C. Board Schematics	7-1
7-2	Font Memory P. C. Board Schematics	7-4
7-3	Main Logic P. C. Board Schematics	7-5
7-4	I/O P. C. Board Schematics	7-12
7-5	Sync Gen/Encoder P. C. Board Schematics	7-16
7-6	Dual Oscillator P. C. Board Schematics	7-17
7-7	Keytronics Keyboard Schematics	7-18
APPENDIX	Technical Data for Shugart SA300 Disk Drive	2-1
	P/N 39254-2	

SECTION 1

Introduction

1.1 GENERAL

The Chyron VP-2 is a low-cost, high-resolution, single-channel character and graphics generator with features usually found on much more elaborate studio systems. With a completely integrated keyboard and micro-disk drive, the system provides 35-nanosecond resolution, selection from 512 colors, up to six fonts, and multiple character variations.

The VP-2 system functions with the ability to compose and display color video messages for output to an external display. It can be used as a stand-alone character generator, or operate in a downstream or upstream configuration combining external video with VP-2 graphics. Practical applications include video production, industrial training applications, and taped commercial productions. Other applications can include information displays, such as those located in hotels and airports, or business sales projections, financial data, progress charts, product breakdowns or marketing data.

1.2 APPROACH

This manual provides the maintenance technician with sufficient descriptive information to develop a functional understanding of the VP-2 not only as a whole, but to develop further understanding of each major part of the VP-2 structure. The qualified technician will then be able to isolate problems in the VP-2 to individual PC boards within the unit, and either repair the boards or request instructions to ship them to CHYRON for replacement.

The technician should have a basic understanding of electronic circuits and standard test equipment, and be able to handle components, connectors, and printed-circuit boards.

Most failures can be isolated to one of the major assemblies in the VP-2 using standard test equipment and procedures. Most of these problems can be identified and corrected by following simple troubleshooting processes. However, if more complex problems are traced to PC boards, these boards can be removed from the unit and shipped to CHYRON for repair. CHYRON can repair the board and ship by return mail, so the unit's operation is restored in a minimum time.

The following test equipment is required to maintain and troubleshoot the VP-2:

- Digital Multimeter
- Dual-Trace Oscilloscope (100MHz or better)
- Waveform Monitor
- Sync Generator
- Vectorscope
- Non-metallic Adjustment/Alignment Tools

1.3 CONTENT

Section 2 of this manual is an overall functional description of the VP-2, whereas Section 3 provides a more detailed description of each printed circuit board. We recommend that the responsible technician become thoroughly familiar with the content of these two sections. Section 6 contains detailed parts lists, and Section 7 includes schematic diagrams of the various major assemblies.

Section 4 provides the troubleshooting procedures which, in most cases, will enable the technician to determine cause of operational problems. Section 5 provides a detailed video alignment procedure.

SECTION 2

Architectural Overview

The VP-2 character generator system uses pre-programmed character sets (fonts) and digital/analog encoding to produce and manipulate characters and backgrounds. These manipulations include edge and border generation, italicizing, roll, and palette animation. The VP-2 will display any 8 colors simultaneously out of a color palette containing 512 colors. The VP-2 system is controlled by a portable keyboard, and produces NTSC or PAL composite video. The VP-2 contains an internal keying circuit that allows the insertion of graphics over an external video signal. Consult the VP-2 Operation Manual (Pub. No. A-2A0-0679) to become more familiar with the basic functions of the system.

2.1 SYSTEM INTRODUCTION

The components of the VP-2 system may best be described through their functions in the image generation process. Image generation involves processing the display information from the keyboard to produce a digital representation of the desired screen image including font and color data, and from there converting this digital representation into composite video. The procedure can be broken down further into these functional blocks which correspond to printed-circuit boards within the unit (see Figure 2-1 for an overall block diagram):

- Dual-Processor P. C. Board
- Font P. C. Board
- Main Logic P. C. Board
- I/O P. C. Board
- Sync Gen/Encoder P. C. Board
- Power Supply

2.1.1 Dual Processor P. C. Board

2.1.1.1 8088 Microprocessor. The 8088 microprocessor and subsystems (buffer/drivers, latches, etc.) control most data-transfer operations within the VP-2. The 8088 also generates select signals to control the keyboard interface, the disk-drive interface, video address generation, color generation, and all CPU interrupts. The 8088 has exclusive control of the 80186 microprocessor. These CPU's communicate through a shared static RAM memory array. Programming for the 8088 resides on the Main Logic Board in three EPROM devices.

2.1.1.2 80186 Microprocessor. The 80186 microprocessor is a 16-bit device that has direct access to the Font P. C. Board. The 80186 receives commands from the 8088 to fetch font data and to create a digital representation of the desired screen image. This image representation is output to the 8088 CPU in the form of scanline segments (run-length pairs), where it is loaded into the video frame buffers. The programming for the 80186 microprocessor resides in two EPROM chips located on the dual-processor board. The 80186 also uses a dedicated local RAM array.

2.1.2 Font Memory P. C. Board

The Font P. C. Board connects to the dual-processor P. C. board by a 60-wire ribbon cable. The board itself has six zero-insertion force sockets, and chip-select decoding logic. The 80186 addresses the font ROMs on a 15-bit address bus, and receives data on an 8-bit data bus. Four video adjustments are located on the Font P. C. Board. These adjustments are for Coarse Subcarrier Phase, Fine Subcarrier Phase, Horizontal Phase Timing, and Keyer Mix Rate. The Genlock LED is also located on this P. C. board. These adjustments are not electrically connected to the font memory circuitry on the board, but are connected to the Sync Gen/Encoder P. C. Board through a 15-line ribbon cable.

2.1.3 Main Logic P. C. Board

The Main Logic P. C. Board combines the digital information of the screen image with data from the color palette to produce the final digital representation of the video. This information is stored in frame buffers located on the board, and is output to the Sync Gen/Encoder P. C. Board, where the information is converted into actual composite video. The functions of the Main Logic Board are all controlled directly by the 8088 CPU. These functions may be broken into the following subsystems.

2.1.3.1 Memory. The Main Logic Board has four areas of memory. These may be divided into program memory, scratch memory, palette memory, and video memory. Three EPROM devices are used for program memory; three IRAM devices are used for scratch memory; three static RAM devices are used for palette memory; and 32 static RAM devices are used for video memory.

2.1.3.2 Color Generation. The Main Logic Board generates the color data specified by the operator. All colors in the VP-2 system are made up of varying levels of red, green, and blue. These levels are specified as three-bit quantities, which correspond to an intensity of 0 through 7 for each color. Up to eight colors can be displayed at any given time. The palette RAM stores the color information that is generated by the 8088 in this form.

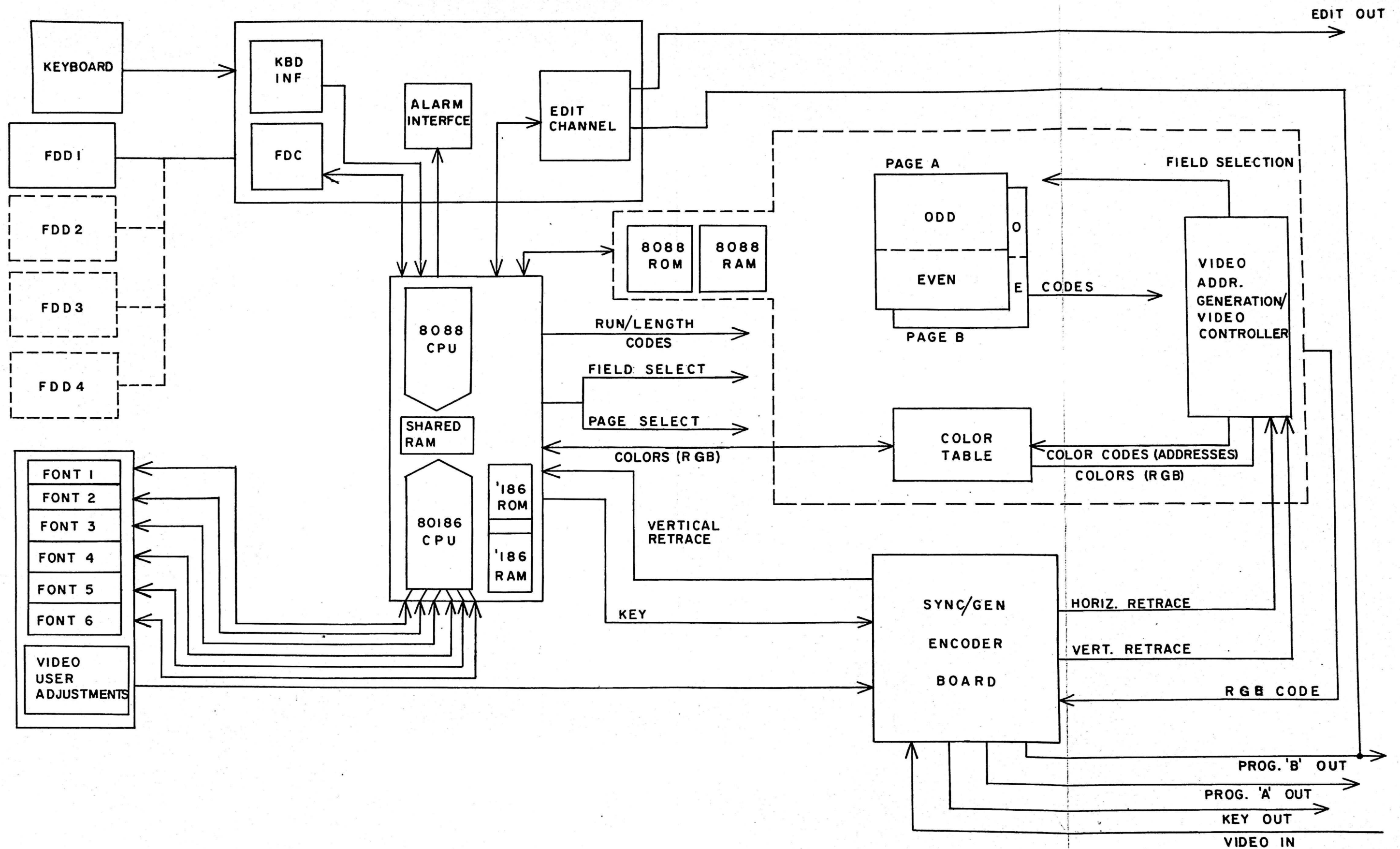


Figure 2-1. VP-2 Character Generator Functional Block Diagram

2.1.3.3 Video Address Generation. Video address generation creates the pages and fields used to display VP-2 graphics. In raster video applications there are two fields to every frame (one odd field and one even field). The VP-2 generates two pages (of two fields each) to create the desired video image.

Video start addresses are read from the CPU data bus and are divided into odd-field addresses and even-field addresses. These addresses are used to determine the scan-start pointers, which are used by binary counters as starting addresses. These address counters increment the video addresses one by one, timed to the system bit clock signal.

2.1.3.4 Video Controller. The video controller logic generates the selection and synchronization signals used elsewhere in the video generation process. The circuitry must also select pages and fields within the frame buffers, and perform the switching between image generation and video generation. The video controller also decodes the run-length information into color selections and scanline segment lengths.

2.1.4 I/O P. C. Board

The I/O P. C. board performs four functions for the VP-2 system. The board holds the keyboard interface, alarm interface, edit channel circuitry, and floppy-disk controller circuitry.

2.1.4.1 Keyboard Interface. The keyboard itself contains a microprocessor and its own source of programming that sends serial data to the interface. The keyboard interface translates keystrokes into digital information for the VP-2. This data is converted into parallel data by the interface, and output to the Main Logic Board.

2.1.4.2 Alarm Interface. The VP-2 uses a piezo-electric beeper to register errors or to inform the operator of particular conditions. The alarm interface consists of decoding logic and a monostable multivibrator (one-shot) that converts a combination of signals into a single pulse for the beeper.

2.1.4.3 Floppy-Disk Controller. The floppy-disk controller circuitry enables the VP-2 to write to, read from, search, and address a floppy disk. The FDC, like the keyboard, contains a microprocessor and its own source of programming. When writing to the disk drive, the FDC converts VP-2 data into the encoded form that is stored on the disk. When reading, the FDC converts this encoded data into serial data for the VP-2. All disk-drive controls are handled through the FDC.

2.1.4.4 Edit Channel. The edit channel circuitry produces the on-screen menus, text, and cursor present at the "Edit Out" connector. The video display processor (VDP) receives menu and text data from the Dual Processor Board, combines this with composite video taken from the Sync Gen/Encoder Board, and outputs the keyed video signal directly to the VP-2 back panel. The VDC contains its own programming, and uses a separate block of video RAM.

2.1.5 Sync Gen/Encoder P. C. Board

The Sync Gen/Encoder contains logic to address and read bytes from VRAM, retrieve the proper color data from palette RAM, convert the digital information into analog levels, and to finally convert the analog levels into composite video. The Sync Gen/Encoder contains these functional blocks:

- Digital Encoder
- Video Mixer
- Keyer Control
- Genlocking Timing Generator

2.1.5.1 Digital Encoder. The Digital Encoder converts the 3-bit RGB signals from the Main Logic Board into equivalent 8-bit YUV signals. These signals are then converted into analog form as either NTSC or PAL composite video.

2.1.5.2 Video Mixer. The Video Mixer provides a means of combining the signal on the Video In channel with the insert video signal generated by the digital encoder. The insert video is keyed over the VIDEO IN signal which appears as the background signal.

2.1.5.3 Keyer Control. The video mixer control signals are provided by the Key Control circuitry. The key signal amplitude is controlled by a variable speed ramp generator to allow adjustment of the keyer mix rate. Additionally, a video-level Key Out signal is produced for use with external keyers.

2.1.5.4 Genlocking Timing Generator. The Genlocking Timing Generator provides timing signals for the entire system in both the stand-alone and Genlock configurations. The Genlock circuitry is designed to accommodate a wide range of input timing discrepancies and allows adjustment of horizontal phase timing and subcarrier phase.

2.1.6 Power Supply

The power supply is mounted on a separate printed circuit board. On the AC side, the supply runs on 115 VAC, and consumes approximately 100 watts. The AC power line is fused with a 3-amp cartridge fuse located on the VP-2 back panel. The power supply outputs are Ground, -12 volts, +12 volts, and +5 volts.

2.2 IMAGE GENERATION

The VP-2 image generation process requires a very high pixel resolution (35 ns/pixel) to produce video displays suitable for NTSC or PAL presentation. Due to the memory limitations of the VP-2 hardware, the run-length encoding method is the display method of choice. Run-length encoding entails the specification of the characteristics of individual portions of scanlines in terms of (color, length) byte pairs.

The approach to color taken in the VP-2 architecture allows the display of up to 8 colors simultaneously out of a 512-color palette. The "color" term of the run-length pair is a 3-bit quantity (000_2 - 111_2 or 0 - 7 decimal) that represents an address into a table of colors. Thus, the number of displayable colors is eight, but the number of available colors is only limited by the width of the color table. In the VP-2, the color table is 9 bits wide, which is divided into 3 bits for each of the primary colors red, green, and blue.

2.2.1 Run-Length Encoding

Run-length encoding is a method of video display that uses a series of 8-bit words to specify segments of scanlines. The run-length data word contains a 3-bit "color" term and a 4-bit "length" term. The "length" term may be viewed as a "count" term, which counts the number of pixels that will appear in the specified color.

NOTE: Due to an architectural characteristic of the video generator, the number of pixels displayed in the specified color will actually be "count" plus one (count+1). Thus, the minimum length that may be specified is two pixels, since specifying a "count" of zero denotes an end-of-line or end-of-field code.

Due to the length of a scanline (1510 pixels, not counting overscan for NTSC; 1430 pixels, not counting overscan, for PAL) it is not possible to encode a scanline into a single byte. In fact, the VP-2 requires several bytes to specify a maximum length scanline run. Therefore, the VP-2 architecture recognizes two types of run-length codes: transition codes and continuation codes. The eighth bit denotes the type of code.

2.2.1.1 Transition Code. Transition codes are used to indicate changes in the color of a scanline. This code indicates that the scanline is to assume the specified color for the specified "count" of pixels. A transition code is denoted by a "1" located at the eighth bit. See Figure 2-2 for the format of a Transition Code.

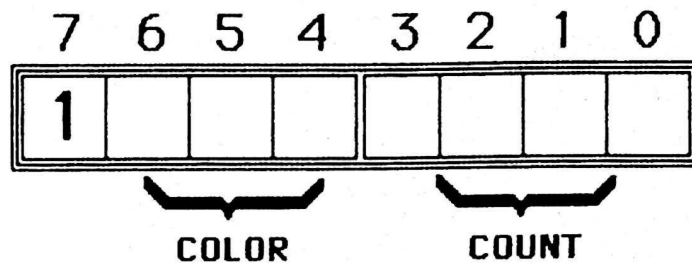


Figure 2-2. Transition Code Format

2.2.1.2 Continuation Code. Since the 4-bit "count" element of a transition code is severely limited in length, continuation codes are necessary to allow longer portions of scanlines to be specified. The continuation code specifies a number of pixels to be drawn on the screen in whatever color is currently active (i.e., whatever color was last specified in a transition code). A continuation code is denoted by having a 0 in the location of the eighth bit of the word. See Figure 2-3 for the format of a continuation code. Note that the same restriction applies to this "count" as to the transition code "count" (see NOTE on page 2-7).

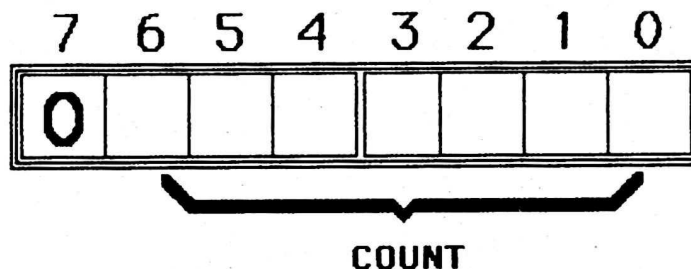


Figure 2-3. Continuation Code Format

2.2.1.3 End-of-Scan/End-of-Field Codes. When the END-OF-SCAN code ("count" = 0) appears as the first code for a scanline, it indicates END-OF-FIELD, meaning that the remainder of the field will appear as the last specified color.

2.2.2 Frame Buffer

The VP-2 frame buffer holds a representation of an entire screen image. The 8088 writes its run-length data into this area, and the Sync Gen/Encoder reads from this area to produce the video image. To allow updating of the screen image, the VP-2 is "double-buffered," meaning that two identical frame buffer memories are provided, with the video section reading from one buffer while the image generator is writing into the other. Thus, new images may be generated without affecting the image being displayed.

Each frame buffer is divided into two fields. These fields correspond to the two fields of an interlaced video display, the ODD field and the EVEN field. Therefore, both the image generator and the video section write or read data from alternating portions in the frame buffer. Thus, the frame buffer is divided into four distinct areas of memory: two image buffers (called "pages" in VP-2 terminology) and two field buffers (odd and even) within each page. Access to the various buffers is controlled through selection signals generated by whichever section (image generation or video section) is using the buffer.

2.3 VIDEO GENERATION

The Video Generation function of the VP-2 produces the final video image from the run-length information written into the frame buffer by the image generator. The video generator must select the proper frame buffer, read the run-length codes from the frame buffer, and produce the specified scanline segments on the screen. The video generator repeats its function for each field in the video display, or 60 times per second. Selection between field buffers is performed as each field is displayed.

The starting point of the video generator's scan is controlled by the image generator through a pair of scan start pointers, one per field. The video generator will begin its scan for a field at the address contained in that field's scan start pointer, and will scan for as long as required to complete the field. A wrap-around feature of memory addressing allows for pointer manipulation which facilitates such features as roll.

SECTION 3

Functional Theory of Operation

3.1 DUAL-PROCESSOR BOARD

The Dual Processor Board contains the 8088 and 80186 microprocessors, and the circuitry necessary for their operations. The Dual Processor Board communicates with the rest of the VP-2 through a 40-pin DIP connection to the Main Logic Board, an SBX data bus connector, and through a 60-wire ribbon connector to the Font P. C. Board.

The CPUs communicate through a dual-port static RAM array (U22 and U23). Since only one CPU can access the shared RAM array at any given time, access is controlled through an arbitration circuit. The arbitration circuitry is based around D-flip/flop U38; contains multiplexers U26, U27, U31, and U32; and octal bus transceivers U12, U13, U15, and U16. Since the shared RAM is an integral part of each CPU interaction, in descriptions the shared RAM will be viewed as transparent. In order to facilitate understanding of the various functions of the dual processor board, each CPU and its associated circuitry will be discussed individually. Refer to Figure 3-1 for a functional Dual Processor P. C. Board Block Diagram.

3.1.1 80186 CPU

The Intel 80186 microprocessor is a 16-bit device that performs two major VP-2 functions. The 80186 accesses font information from the Font P. C. Board through a 60-wire ribbon cable. This ribbon cable carries 15 address lines, 8 data lines, 3 chip select lines, and an 80186 read enable signal. (See paragraph 3.2 for a functional description of the Font P. C. Board.)

The 80186 also performs the image generation function for the VP-2. The 80186 receives screen command data from the 8088 CPU and accesses the required font information from the font PROMs. With this data, the 80186 generates a model of the desired video image, and outputs this data in the form of run-length pairs (scanline information) to the 8088, which in turn loads the scanline data into the VRAM.

3.1.2 8088 CPU

The 8088 CPU is an 8-bit device that performs all data transfer and control functions within the VP-2. The 8088 produces many of the internal control signals for the VP-2, and also controls most aspects of the video generation processes. The 8088 reads user information from the keyboard interface on the I/O board, and compiles this information into a text buffer.

Information from the text buffer is sent to the 80186 CPU to access font information to create the desired image. The 8088 also reads from and writes to the floppy disk through the floppy-disk controller on the I/O board. Color palette information is controlled by the 8088 CPU in the form of RGB values, stored in RAM on the Main Logic Board. The 8088 then uses information from the 80186 and from the color tables to produce the final image of the video frame, which is output to the frame buffer on the main logic board, which in turn is converted into actual video by the Sync Gen/Encoder board.

The 8088 CPU directly controls the video display processor (VDP) of the Edit Channel. Due to software architecture, the edit channel menus are stored in the 80186 program space. The 8088 accesses menu information from the 80186, and outputs this information to the VDP. (Paragraph 3.4.4 contains a detailed edit channel description.)

3.2 FONT MEMORY P. C. BOARD

The Font Memory P. C. Board can accommodate up to six PROM font memory chips, and contains decoding logic to produce chip select/enable signals for each font. The Font Memory Board communicates with the Dual Processor Board over a 60-line ribbon connector.

PROM U1 reads the three highest address bits from the 80186 CPU and generates the six chip select signals necessary for the Font Memory board. The 80186 CPU's address bits $A_0 - A_{13}$ are used to access font data.

The Font Memory Board also contains four video adjustments. These adjustments are connected directly to the Sync Gen/Encoder board by J2 and a 15-line ribbon cable, and they have no electrical connection to the rest of the Font Memory circuitry. These adjustments are Coarse Phase Adjust, Fine Phase Adjust, Horizontal Phase Timing, and Keyer Mix Rate. The Genlock LED is also located on the Font Memory board, near the other video adjustments. Refer to paragraph 5.3 for more information about these adjustments. See Figure 3-2 for a functional block diagram of the Font Memory P. C. Board.

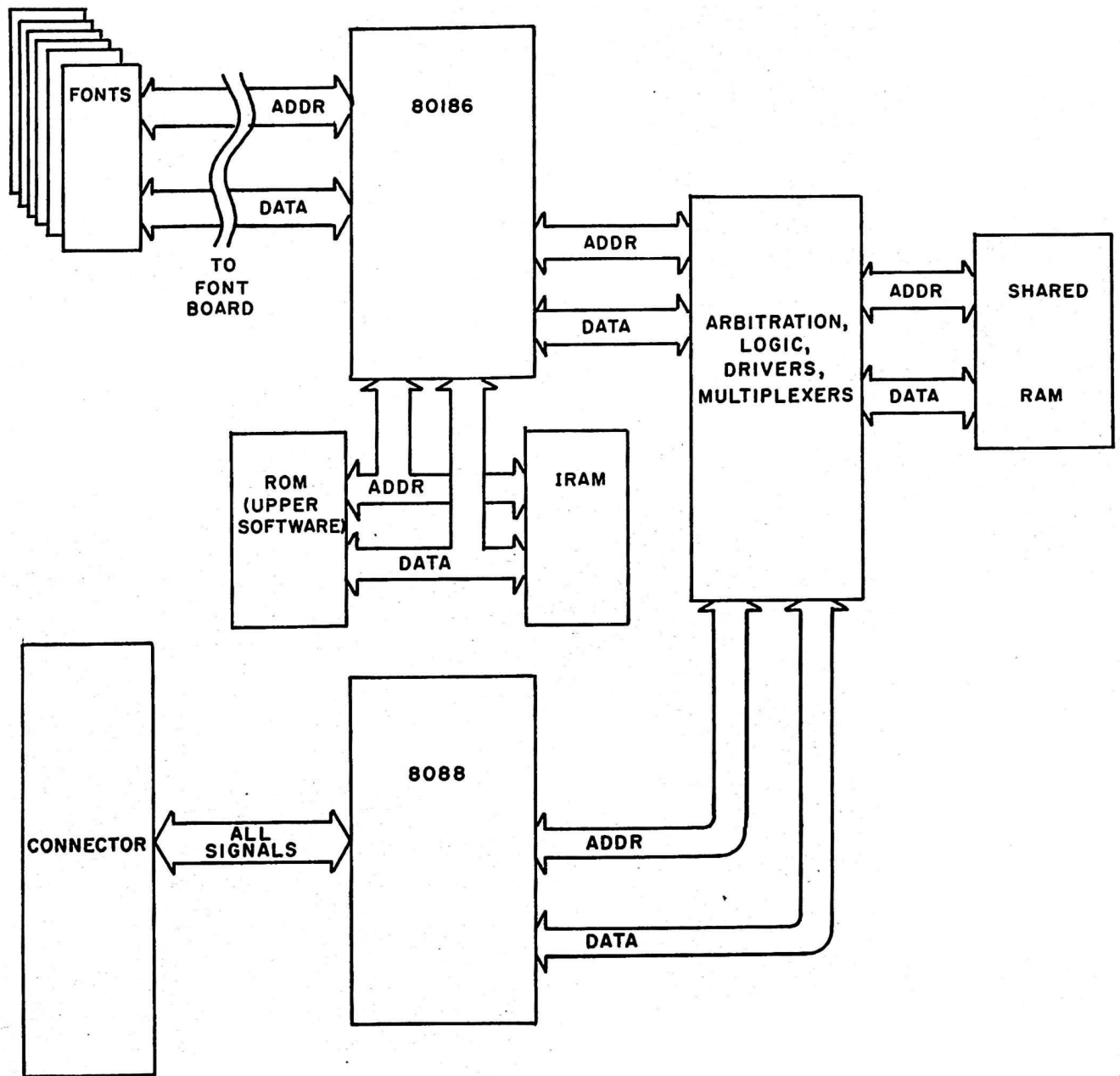


Figure 3-1. Dual Processor P. C. Board Block Diagram

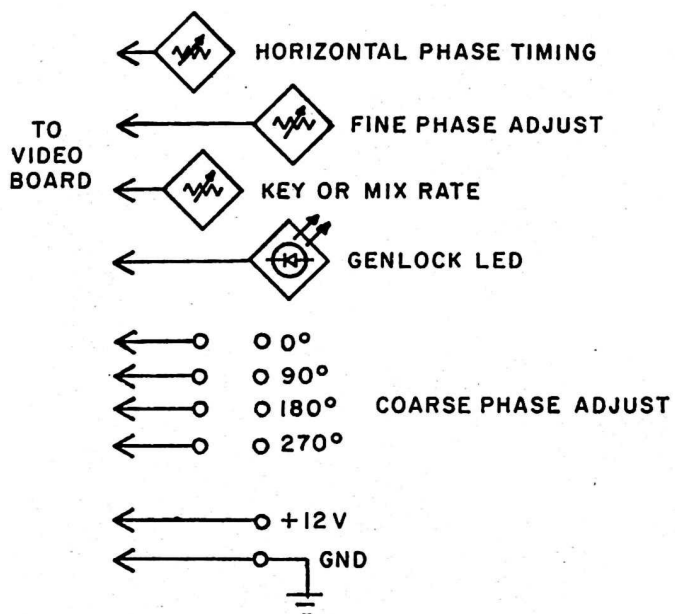
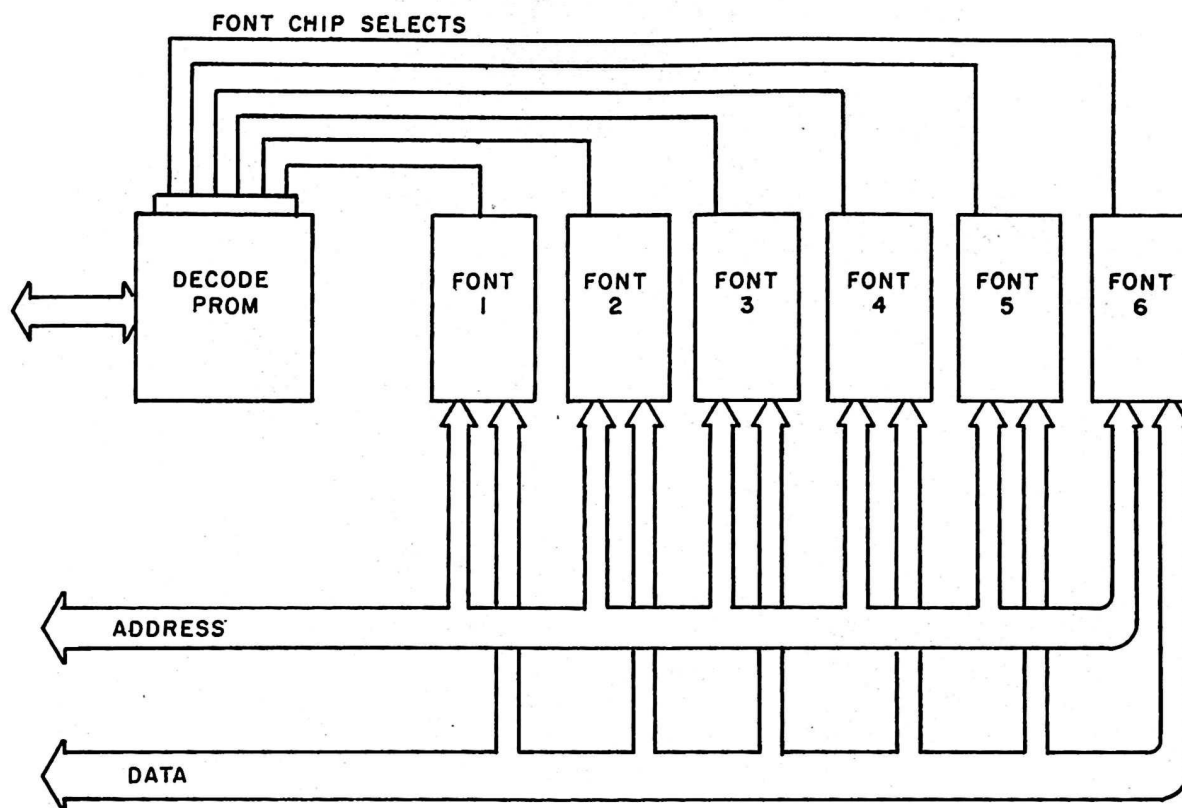


Figure 3-2. Font Memory P. C. Board Block Diagram

3.3 MAIN LOGIC P.C. BOARD

The Main Logic P. C. Board combines the digital image of the desired screen image with data from the color palette and produces the final digital representation of the video image for the Sync Gen/Encoder P. C. Board. This information is stored in the frame buffer located on the board, and is output through a video controller to the Sync Gen/Encoder P. C. Board, where the information is converted into actual composite video. The functions of the Main Logic Board are all controlled directly by the 8088 CPU. Figure 3-3 is a complete block diagram of the Main Logic P. C. Board. The Main Logic P. C. Board may be broken into the following subsystems:

- Address Latch and Data Multiplexers
- Chip Select/Enable Logic
- Memory Systems
- Color Generation
- Video Address Generation
- Video Controller Circuitry
- Keying Logic

3.3.1 Address and Data Buses

The 8088 CPU uses a 18-bit address bus and an 8-bit data bus. The address bus is divided into the low-order bits $A_0 - A_7$ and high-order bits $A_8 - A_{17}$. The address bus is latched into two 8282 8-bit address latches, U92 and U113. The 8-bit data bus generated by the 8088 has sufficient drive for the VP-2 architecture, and does not require buffering.

3.3.2 Chip Select/Enable Logic

The chip select logic on the Main Logic Board converts signals from the low-order address bus ($A_0 - A_7$) into chip selects/enables for the entire system. The chip select circuitry consists of three decoder/demultiplexer chips U67, U111, and U112.

3.3.3 Memory Systems

The Main Logic P. C. Board contains four specific memory subsystems. These are ROM for the 8088 CPU (U90, U91); RAM for the 8088 (U61 and U89); Shared RAM for the 8088 and 80186 CPUs (U22, U23, on the Dual Processor Board); Palette RAM, which stores data for the color table (U76, U77, U78); and Video RAM, which is a static RAM array that stores a dual representation of the video image (U1 - U7, U10 - U17, U20 - U27, U29 - U36). Refer to Figure 3-4 for a complete VP-2 memory maps.

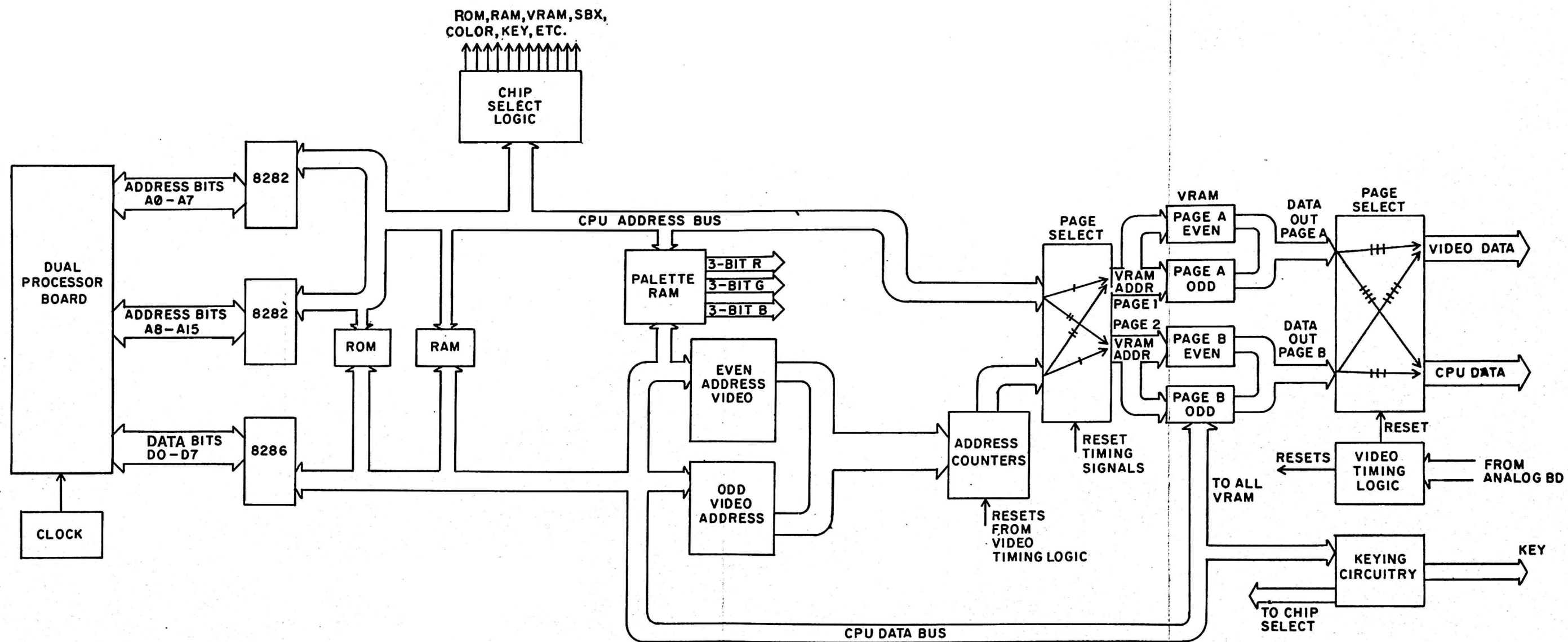


Figure 3-3. Main Logic P. C. Board
Functional Block Diagram
3-5/3-6

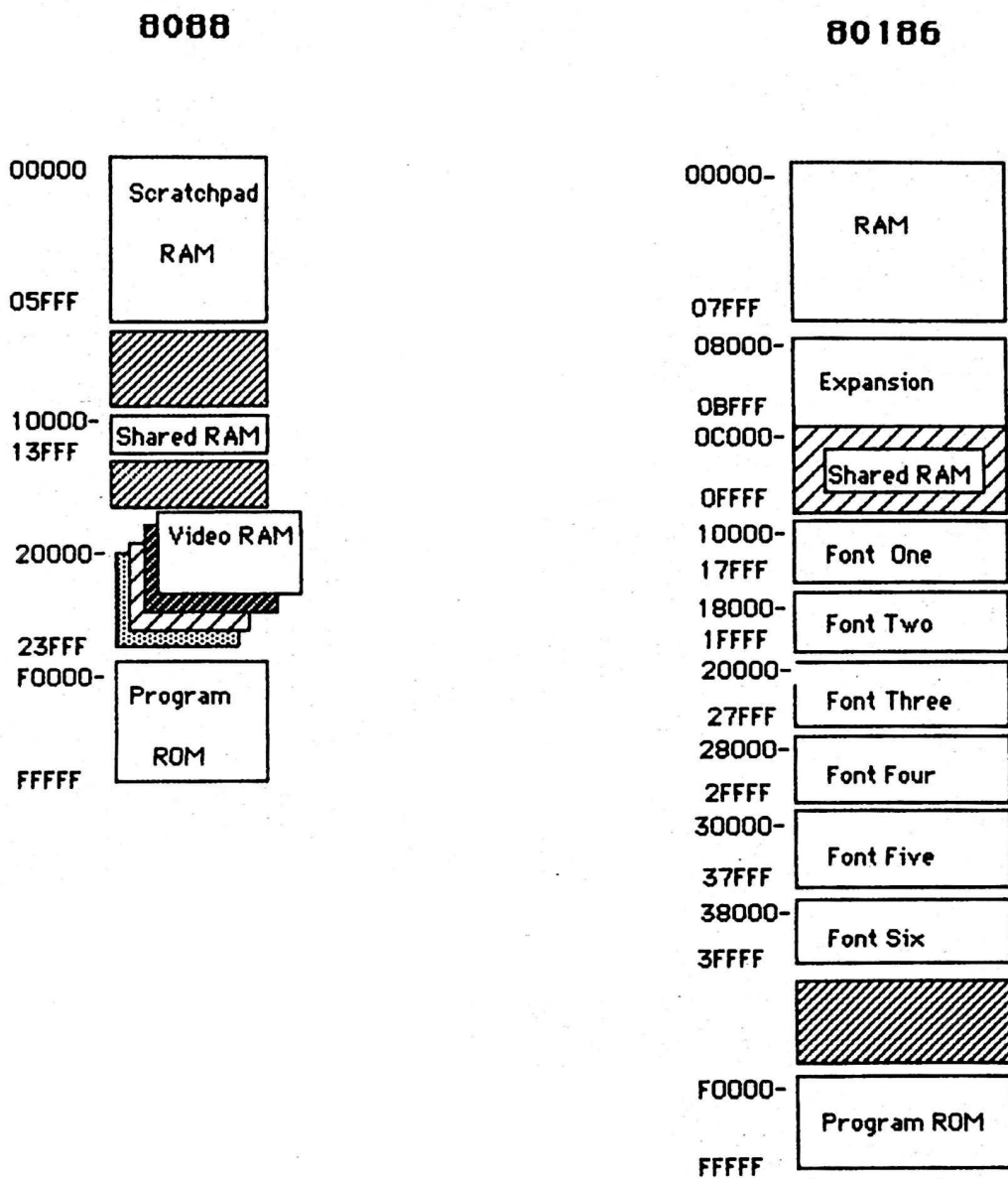


Figure 3-4. VP-2 Memory Map

3.3.4 Color Generation

Colors for video display are generated by the 8088 CPU and stored as 3-bit quantities in Palette RAM. Each one of the eight on-screen colors consists of three 3-bit intensities for each of the primary colors red, green, and blue. Thus, the VP-2 can display any 8 colors out of a possible 512.

In order to load new color data into the Palette RAM, the CPU must first generate chip selects in turn for each of the affected RAMS, which store values for the primary colors. Once the CPU has selected a RAM chip, the data bus writes the new data into the chip.

Each scanline segment consists of a (color, length) pair as data. The "color" term is a 3-bit quantity that corresponds to one of the eight possible on-screen colors stored in Palette RAM. When each scanline segment is being sent to the Sync Gen/Encoder Board, the "color" term is used to address the Palette RAM, which then outputs the desired 9 bits (three 3-bit terms, for each of the primary colors) to be encoded into video.

3.3.5 Video Address Generation

Video start addresses are read from the CPU data bus and are divided by a series of octal flip-flops (U39, U40, U50, U51) into odd-field addresses and even-field addresses, corresponding with the odd and even fields of an interlaced raster video scan.

These addresses are used to determine the scan-start pointers, which are used by binary counters U41, U42, U52, and U53 as starting addresses. The address counters increment the video addresses by one, timed to the system clock signal. Due to an architectural characteristic of the VP-2, memory addresses perform automatic wrap-around when incrementing. Thus, when an attempt is made to address beyond the upper boundary of the frame-buffer logical address space, the address will "wrap-around" to the appropriate location within the buffer. For example, if the buffer resides within the address range $0 - 4000_{16}$, an attempt to address location 4003_{16} will actually reference location 0003_{16} . This feature facilitates such frame manipulations as roll.

3.3.6 Video Controller

The video controller logic generates the selection and synchronization signals used elsewhere in the video generation process, and decodes the run-length information into color selection and scanline segment length. The circuitry must select frame buffers, depending on whether the buffers are being accessed by the image generator or the video generator. The video controller logic must also select alternating fields within each frame buffer to create interlaced raster video. The logic also synchronizes the page- and field-select functions to the system clock. Other functions of the video controller circuitry include detecting and decoding specialized run-length codes such as continuation code and end-of-line or -field codes.

3.3.7 Key Controller

When the operator selects a "key color," one of the eight on-screen palette addresses will be keyed over and an external video signal will show in its place. The circuitry that performs this is related to the color generation circuitry discussed previously in paragraph 3.3.4.

The key color circuitry monitors the addresses that are being selected by the image generator for scanline segments. The keying circuitry latches the "color" term of the scanline segment being produced in 4-bit latch U70 and then compares the 3-bit "color" term of the scanline segments with a 3-bit representation of the key color address in comparator U81. Whenever the two values are equal, the key controller logic produced a keying signal, which is used on the Sync Gen/Encoder Board to switch between the internally generated VP-2 graphics and an external video signal.

3.4 I/O BOARD FUNCTIONAL DESCRIPTION

The I/O P. C. board contains four subsystems and decoding logic to provide four functions to the VP-2 system. These functions consist of a Keyboard Interface, Alarm Interface, Edit Channel circuitry, and Floppy-Disk Controller. The I/O Board communicates with the rest of the VP-2 system through a 36-pin SBX bus connector. Refer to I/O Board Block Diagram, Figure 3-5.

The SBX connector carries the following signals:

PIN #	SIGNAL NAME
5	RESET
6	CLK (28 MHz clock signal from Video Board)
33	D0
31	D1
29	D2
27	D3 (8-bit data bus)
25	D4
23	D5
21	D6
19	D7
11	A0
9	A1 (3-bit address bus)
7	A2
20	CS0
22	CS2 (four-chip select signals)
24	CS4
10	CS6
12	INT0 (two system CPU interrupt lines)
14	INT1
15	IORD (read pulse, write pulse)
13	IOWRT
1,2	power
35,3	ground

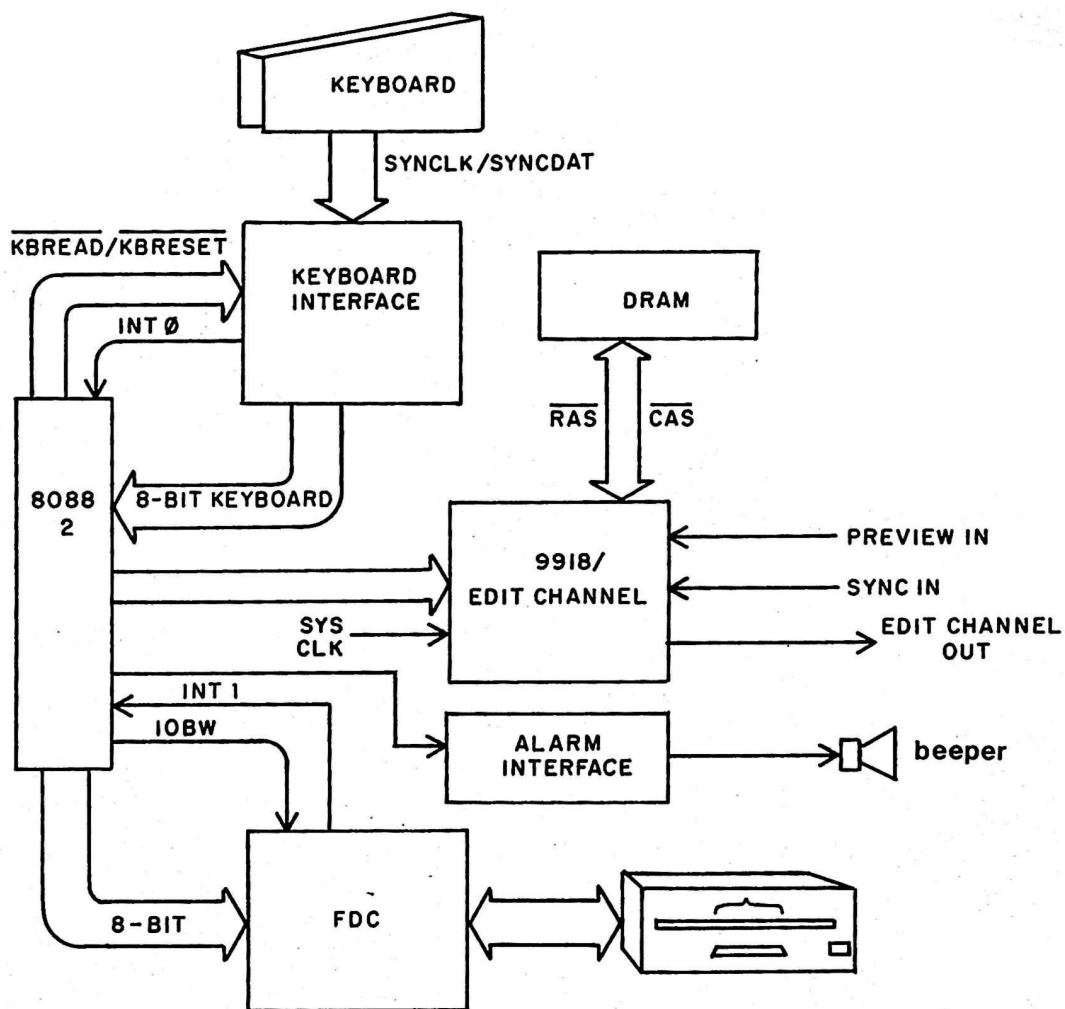


Figure 3-5. I/O Board Functional Block Diagram

3.4.1 Decoding Logic

The decoding logic for the I/O board consists of the inverting buffers U15 and U16, the NOR gates U34 and U35, and the OR gate U31. The input signals used by the decoding logic consist of the address lines A₀ - A₂; the chip-selects CS₀, CS₂, CS₄, CS₆; the IORD and IOWRT pulses; and the RESET pulse.

Outputs from the decoding logic are READ KEYBOARD, RESET KEYBOARD, FDC RESET, ALARM, and 9918 READ/WRITE.

3.4.2 Keyboard Interface

The VP-2 keyboard contains a separate microprocessor and its own programming. Keyboard data are generated at the keyboard as 8-bit serial quantities, and are sent directly to the I/O board keyboard interface accompanied by a clock pulse (which acts as a read window for the serial data).

The keyboard data and clock signals are input to pins 2 and 14 of RS422 line receiver U13. These signals are buffered and then input to serial data input D_{S7} (pin 18) and clock pulse input CP (pin 12) of shift/storage register U32. U32 converts the 8-bit serial data to parallel data which are output through parallel output pins I/O₀ - I/O₇. As soon as the keyboard data are de-serialized, the Mode Select S₁ (pin 19) is forced low, causing U32 to go into the HOLD mode to prevent more data from being sent by the keyboard. Simultaneously, Q₀ (pin 8) goes high, causing D-flip/flop U33 to send an interrupt (INTR₀) to the 8088 CPU. The 8088 then reads the parallel data from the U32 data outputs, and then sends a reset pulse to both U32 and U33, allowing more data to be sent from the keyboard. See Figure 3-6 for a detailed block diagram of the keyboard interface.

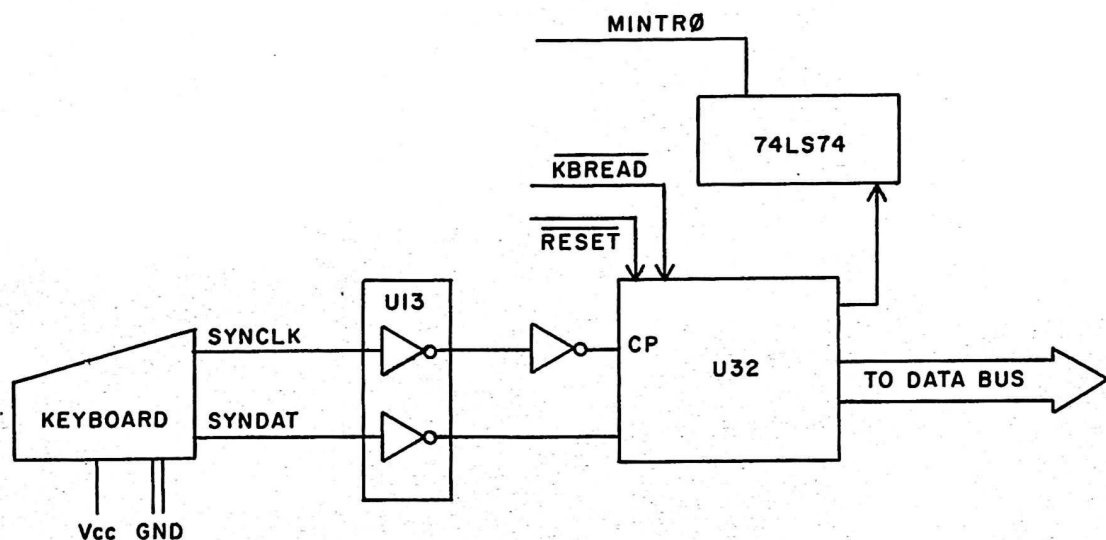


Figure 3-6. Keyboard Interface Block Diagram

3.4.3 Alarm Interface

The alarm interface circuitry is controlled by the 8088 CPU through the decoding logic. The IORD, IOWRT, and MA0 signals are input from the SBX bus to three-input NOR gate U34 and then to inverting buffer U16. The resulting alarm pulse is input to a monostable multivibrator (one-shot) circuit consisting of U30, with time constants R32 and C21. Upon receiving the alarm pulse, the one-shot circuit sends a pulse of length determined by the time constant to a piezo-electric beeper. See Figure 3-7 for the functional block diagram of the alarm interface.

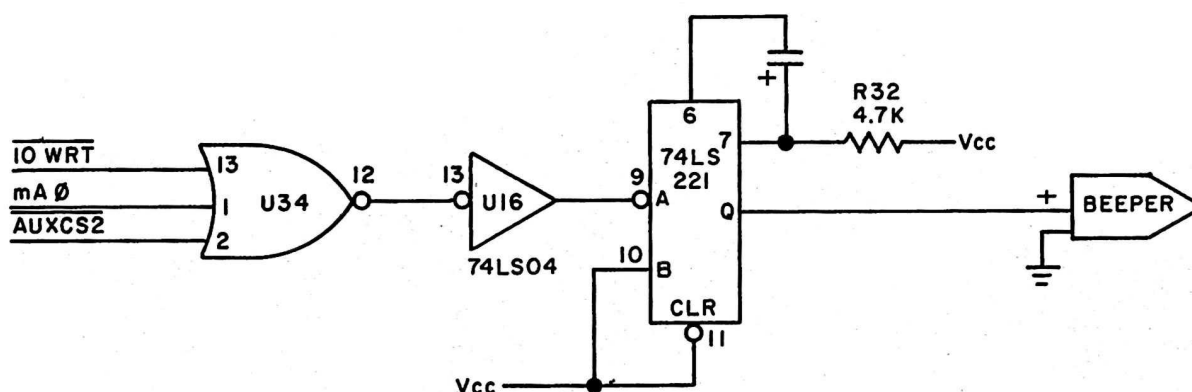


Figure 3-7. Alarm Interface

3.4.4 Edit Channel/Video Display Processor

The edit channel circuitry is based on a VLSI video display processor chip. The inputs for the edit channel system are: Sync In, Preview In, IOWRT, 9918CS, IORD, the 28 MHz system clock (SYSOSC) and the SBX data bus. The outputs of the 9918 are RAS/CAS, R/W, VRAM address bus, and TV OUT.

The SYNC IN signal is taken from J4 pin 8 through a Sync Level Shifter, which pulls the sync level to the chip requirement of +12 volts. The sync signal is then input to pin 34 of the 9918 chip.

The PREVIEW IN signal is taken from J4 pin 5 through an Input Video Balancing circuit. The balancing circuit contains edit channel black-level adjust potentiometer R20. The video signal level is pulled up to +12 volts, and is input to pin 35 of the 9918.

The SYSOSC (28 MHz) is input to pin 2 of U14, which divides it by a factor of 5/2, resulting in the 9918 clock frequency requirement of 10.7 MHz. The signal from U14 does not have a 50% duty cycle, so the clock is run through a LC network and is buffered and driven by Q8 and Q9. The clock signal is then input to inverting buffer U15, where the signal is split into two signals, Ø1 and Ø2. These signals are input to 9918 pins 40 and 39, respectively.

The type and direction of data transfers are controlled by the 9918RD, 9918WR and MAØ inputs from the SBX bus and the decoding logic. 9918WR is the CPU-to-VDP write select. When it is active (low), the 8 bits on MDØ - MD7 are strobed into the VDP. 9918RD is the CPU-from-VDP read select. When it is active (low), the VDP outputs 8 bits on the data bus (MDØ - MD7) to the CPU. MAØ determines the source or destination of a read or write data transfer, and is tied to the 8088 CPU low-order address bit.

The 9918 uses eight 16K x 1 bit dynamic RAM chips as dedicated VRAM. Because of the access frequency required by the 9918, no DRAM refresh/controller circuitry is necessary for proper operation. The VDP VRAM interface consists of two unidirectional 8-bit data buses and three control lines. The VRAM outputs data to the VDP on the VRAM read data bus (RDØ - RD7). The VDP outputs both the address and data to the VRAM over the VRAM address/data bus (ADØ - AD7). The VRAM row address is output when RAS is active (low). The column address is output when CAS is active (low). Data is output to the VRAM when R/W is active (low).

The VDP outputs keyed video containing the VP-2 preview signal plus the edit-channel text, including the VP-2 cursor, on pin 36. This TV OUT signal enters a discrete monitor driver circuit to bring the voltage up to NTSC standards. This signal then leaves the I/O board at J4 pin 2, and goes directly to the "Edit Out" connector on the VP-2 back panel.

Refer to Edit Channel Block Diagram Figure 3-8.

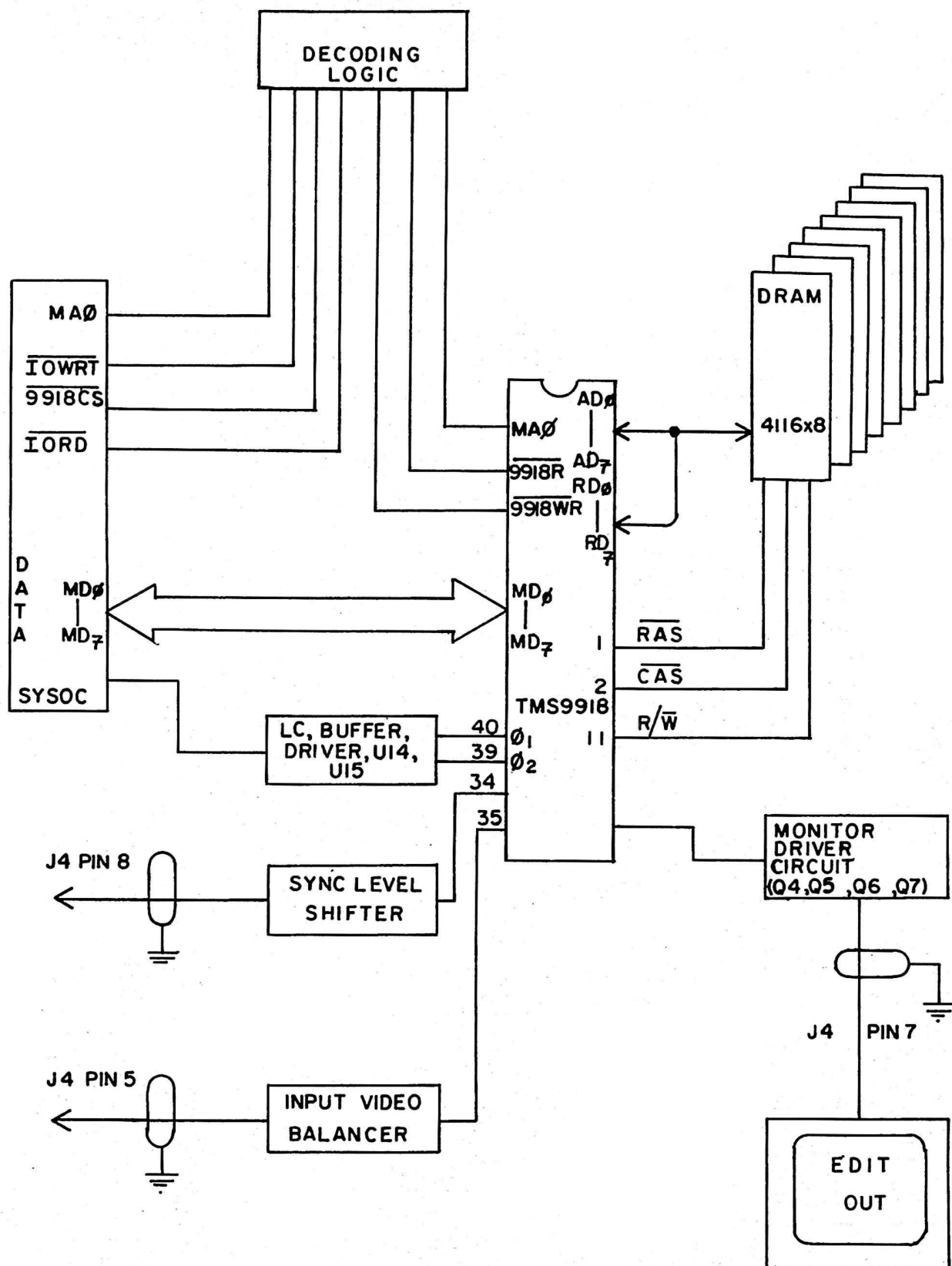


Figure 3-8. Edit Channel Block Diagram

3.4.5 Floppy Disk Controller

The floppy disk controller (FDC) circuitry resides on the I/O P. C. board, and is based on the 8272A floppy-disk controller chip, U28. The FDC communicates with the 8088 CPU through the SBX data bus and is controlled from the CPU by the IORD, IOWRT, RESET, and AUXCS1 logic signals. (Refer To FDC Block Diagram, Figure 3-9; and Appendix for disk-drive unit information.)

The FDC is an intelligent device that performs eight functions necessary for the VP-2 to support data storage and retrieval on up to four disk drives. These functions are READ DATA, WRITE DATA, FORMAT TRACK, SEEK, RECALIBRATE, SPECIFY, SENSE INTERRUPT STATUS, and SENSE DRIVE STATUS.

The CPU sends commands and data on the SBX data bus to the MD₀ - MD₇ (pins 6 - 13) on the FDC chip. The FDC processes command data in three phases: COMMAND READ phase, EXECUTE COMMAND phase, and RESULTS phase. During the Command phase, the FDC accepts up to nine bytes of data from the SBX bus and performs the function specified by the command. Upon receipt of the last byte in the command sequence, the FDC enters the EXECUTE phase. If the command was executed properly (i.e. no error conditions detected), the FDC will interrupt the 8088 CPU and post status information on the data bus.

The FDC communicates with up to four disk drive units along a daisy-chained, open collector interface. The buffered nature of the interface allows drives to be mounted up to 5' away from the controller. Only one drive may be active at any given time on the bus. The drives are selected by one of four drive-select lines, generated by the FDC through drive-select chip U43. The disk drive unit(s) are connected to the I/O board by 34-pin header connector J5.

The FDC requires a 4 MHz clock for internal timing purposes (NCLK) which is provided by 8-MHz oscillator U23, and divided by U17, U18, U19, U20, U21, U24, and U25.

Various control lines are multiplexed by the FDC through U29. Data bytes sent by the CPU are recorded on the floppy disk medium in the form of MFM mode encoded data. Additional logic is provided for write pre-compensation of up to 250 nanoseconds. This logic pre-distorts the written data for certain sensitive patterns described by PS₀ and PS₁ (i.e. the occurrence of two logic-1 pulses in a row may cause an error condition, so the pre-compensating logic intentionally separates the lines). The pre-compensation logic is enabled/disabled by jumper J3.

Encoded data is received from the selected drive at J5 pin 30, and fed into monolithic data separator U22. The data separator constructs a window around the incoming data through which the FDC can identify a valid data string. This retrieved data is then output by the FDC to the SBX data bus.

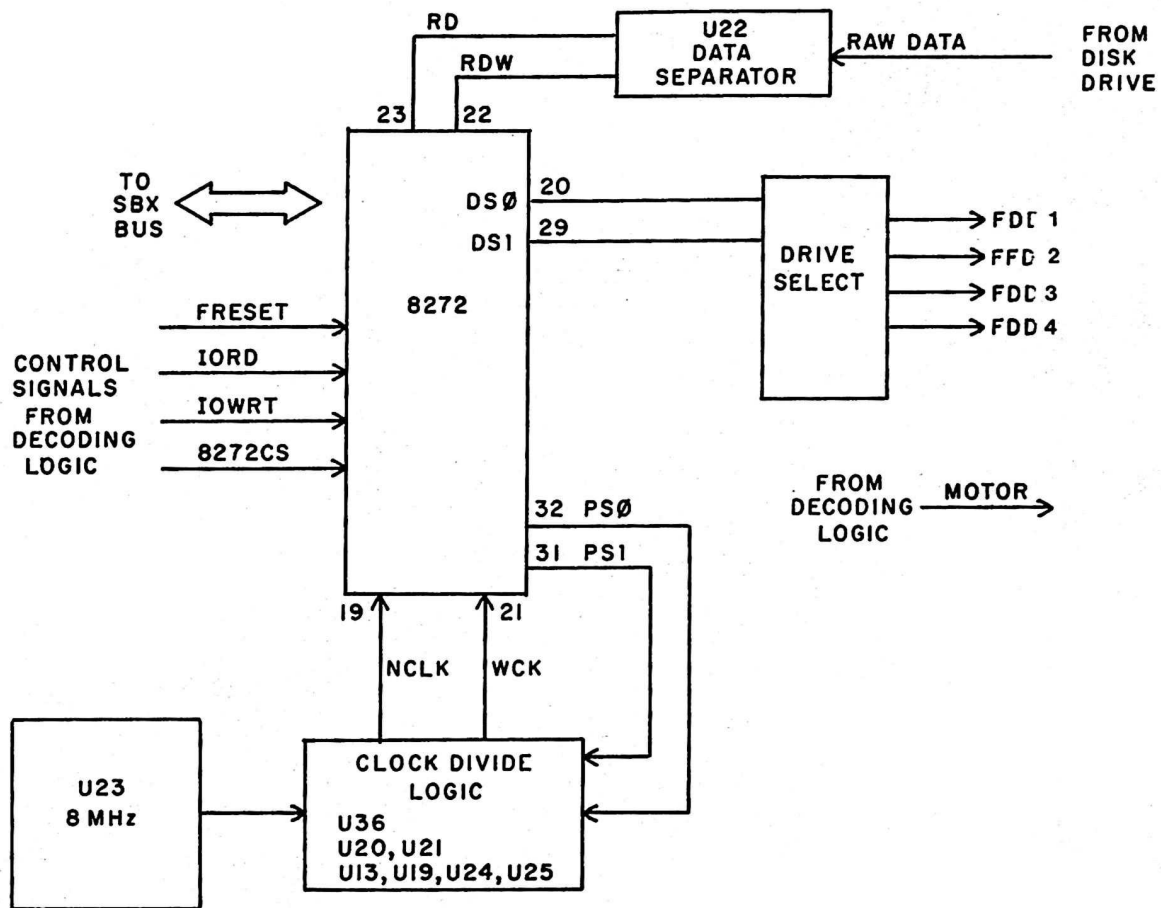


Figure 3-9. Floppy Disk Controller Block Diagram

3.5 SYNC GEN/ENCODER P. C. BOARD

The Sync Gen/Encoder P. C. Board assembly consists of several functional areas. Refer to the Sync Gen/Encoder block diagram, Figure 3-10.

- Digital Encoder: The Digital Encoder converts 3-bit RGB signals from the Digital P. C. Board assembly into equivalent 8-bit YUV signals. These 8-bit values are then converted into analog form and summed to become an NTSC or PAL video signal.
- Video Mixer: The Video Mixer provides a means of combining the Program Input Video with the Insert Video generated by the digital encoder. The insert video is keyed over the program video which appears as the "background" video signal.
- Keyer Control: The Key Control circuitry provides the control signals for the Video Mixer. The circuitry is controlled by the key signal generated on the Main Logic P. C. Board. The key signal amplitude is controlled by a variable speed ramp generator to allow user adjustment of the Keyer Mix rate. Additionally, a video level Key Out signal is produced for use with external keyers.
- Genlocking Timing Generator: The Genlocking Timing Generator provides timing signals for the system in both the stand-alone and genlock modes. The Genlock circuitry is designed to accommodate a wide range of input timing discrepancies, and allows adjustment of Horizontal Phase Timing and Fine Sub-carrier Phase.

3.5.1 Digital Encoder

The nine lines of data from the Main Logic P. C. Board (R1 - R3, G1 - G3, and B1 - B3) are input to the Y, U, V Matrix PROMs U1, U2, and U3. PROM U1 converts the RGB data into an 8-bit number representing the U vector. Similarly, U2 converts the RGB data into an 8-bit representation of the Luminance (Y vector) amplitude, and U3 converts the RGB data into an 8-bit representation of the V vector. Exclusive OR gates U8, U9, U10 and U11 modulate the U and V at the subcarrier rate. Subcarrier blanking is accomplished by gating U and V subcarrier in U12. The burst vector is added in by U5 and U6.

The Y, U, and V data signals are converted to analog form by Digital-to-Analog converters U16, U15, and U14. The current output of U16 is converted to a voltage in the operational amplifier comprised of Q6, Q7 and Q8 and passed to the output summing amplifier Q9, Q10, Q11, and Q12, via Delay line DL1. (The delay line is necessary to match the delay due to the Chroma filter.)

The U and V channel D/A converters are summed together and converted to a voltage in the summing amplifier Q3, Q4, and Q5. The signal then passes through the Chroma filter to the output summing amplifier. The output amplifier combines Luminance, Chrominance, Sync, and Set-Up to form a standard level composite video signal.

3.5.2 Video Mixer

Input video is first clamped by Feedback clamp U23 before passing on to the Program channel of the Video Mixer. The clamp pulse present on U23 pin #5 causes U23 to sample the input video during the back porch interval. The resulting error voltage stored on capacitor C52 is output on U23 pin #6. This voltage is added to the video at the base of buffer Q26 to restore the video component.

The clamped video is applied through R82 to the Program channel of a two-channel video mixer comprised U18, U19, U20, and U22. The mixer is formed by two parallel, two-quadrant transconductance multipliers. Since the multipliers have a non-linear control transfer function, the control signals are pre-distorted by U20 and U22. The Insert video produced by the Digital Encoder is applied to the Insert channel through R69. The control signal from the Key Control Processor is at 0 volt to fully turn on the Program channel and at 5 volts to fully turn on the Insert channel. At intermediate values, a linear mix between the two channels results.

The multiplier output currents are summed together in amplifiers Q20, Q21 and Q22 and are buffered in drivers Q23, Q24, and Q25 to ensure good gain stability and response.

3.5.3 Keyer Control

The Key signal from the Main Logic P. C. Board is input to shift register U4, pins 1 and 2. The shift register is used to delay the key signal to match the encoder delay and to add blanking to the key signal. U7 adds additional delay. U13 is connected as an AND/OR select gate to allow selection between the output of U7 (internal key signal) and an External Key signal. The output of U13 is connected to one input of an Analog AND gate. The other input of the AND gate is the output of U39, the Mix Key integrator. When the output of U39 is low (0 volt) then the key signal is gated off by Q15. When U39 output is high (5.6 volt) the key signal is passed on to the Video Mixer and the Insert Video will be fully keyed over the Program video. At any intermediate voltage range from U39, the key control voltage will be clamped by Q13 to a maximum value equal to U39 output, thus controlling the degree of mix.

D-type latch U34 serves as an alternative action latch (key in/key out) and synchronizer to ensure the key transition is synchronized with the frame rate. The output of U34 pin 8 is low when the key is in and high for key out. On power up the key is forced out by the reset circuit comprised by R184 and C83. When the key is in, FET Q36 is non-conducting and the first section of U39 functions as an inverting amplifier. U39 produces a negative voltage proportional to the Mix Rate voltage, causing the integrator (the second stage of U39) to ramp up. The integrator output is clamped to a maximum of about 5.6 volts by CR5. When the key is out, Q36 conducts and U39 is effective as a non-inverting amplifier, producing a positive output. This positive output causes the integrator to ramp down to about -0.6 volt.

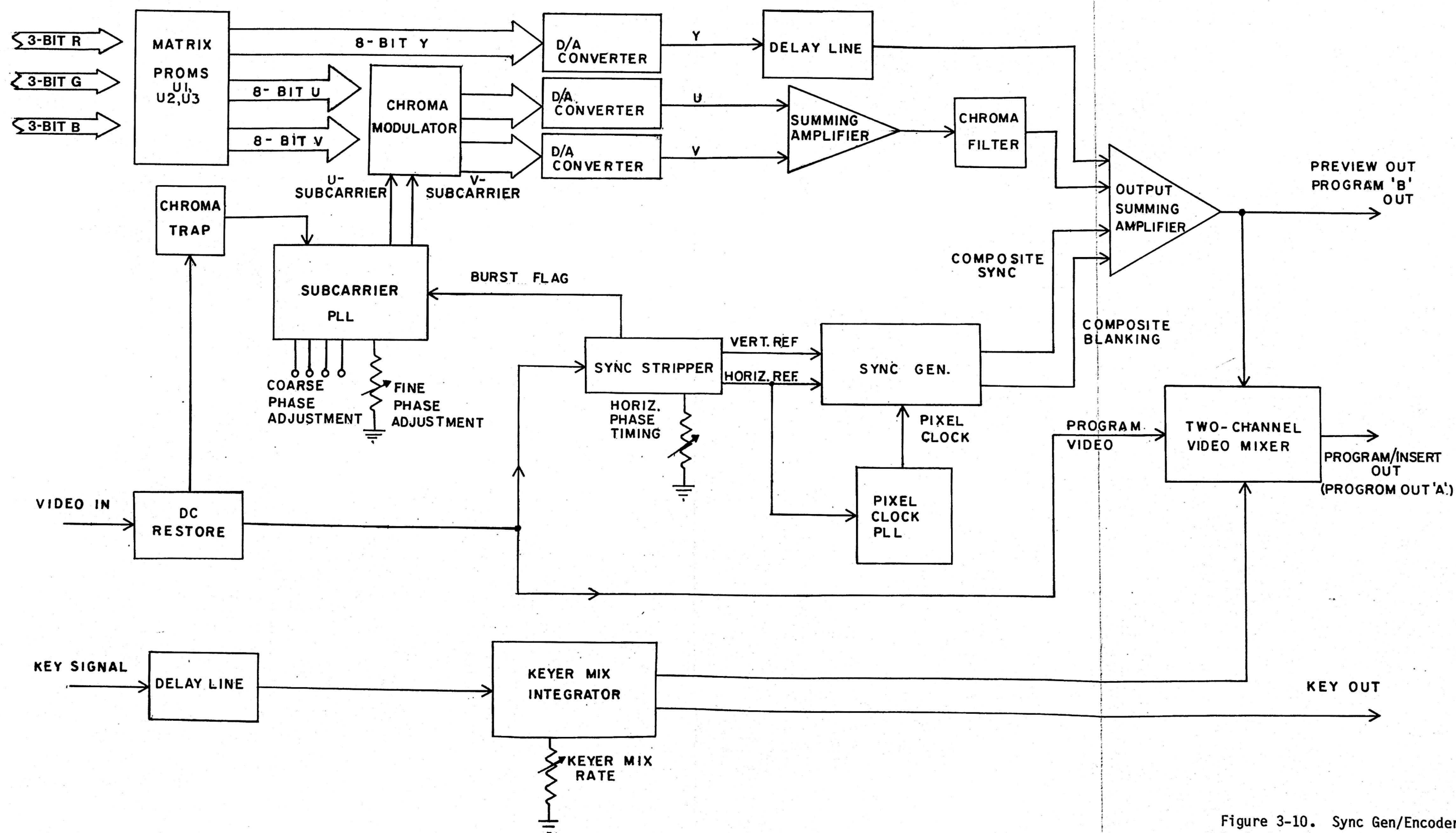


Figure 3-10. Sync Gen/Encoder
P. C. Board Functional Block
Diagram
3-19/3-20

3.5.4 Genlocking Timing Generator

Reference video is input to the sync stripper U24. The first stage of the stripper is an inverting amplifier with a gain of approximately 4. The amplifier is buffered and the inverted video appears at U24 pin 4. The chroma is removed by the chroma trap consisting of C136 and L4, so that the video appearing at U24 pin 4 has a minimum amount of subcarrier remaining. Composite sync derived from the reference (Program Video) appears at U24 pin 1. A clamp pulse is generated by the last transistor in the array U24, and appears at U24 pin 14. The clamp pulse width is determined by the time constant R142 and C52. Reference sync is passed to the vertical sync stripper consisting of U30 and U31. U30 serves to integrate the sync producing a triangular-like waveform only during the vertical sync interval. The triangular waveform is sampled in D-type U31 so that a pulse is produced at U31 pin 6, beginning on the next line after the waveform has crossed the D-type threshold.

The vertical phase adjustment functions by changing the integrator time constant. The vertical rate pulse at TP6 is used to synchronize the timing generator to the reference sync vertical interval.

Reference composite sync (CSP) is also passed to one-shot U29. The timing interval of U29 is approximately 50 μ s so that the twice-line rate sync present during the vertical interval is suppressed. The output of U29 is a horizontal rate waveform that is used as the reference signal for phase comparator U62.

The other input to U62 is supplied by the output of the horizontal phase one-shot U56. This one-shot allows adjustment of horizontal phase with respect to the reference video. U56 is driven by the output of the divider chain comprised of U53, U60, U58, and U57.

The divider takes the output of VCO U56 and divides by 1820 forcing the bit clock (VCO output frequency) to have a frequency of $(1820 * \text{reference horizontal rate})$. U62 output is filtered in low pass filter R232, R231, and C131, buffered by U63 and applied to the frequency control input of the VCO U56.

The divider outputs are connected to the Horizontal Timing PROM U59. The timing signals from U59 are output to the output logic PAL U62 which combines the horizontal and vertical rate pulses to make composite timing signals. PROM and PAL outputs are latched U51.

IC's U49 and U50 are used to produce composite sync, composite blanking, and odd/even field pulses. Vertical rate timing signals are produced by Vertical Timing PROM U44, which is driven by counters U45 and U43. The counter U45 is clocked at twice the horizontal rate derived from the horizontal counter so that 2:1 interlaced sync will be produced. (U41 and U42 are used in PAL systems to provide staggered burst BRUCH blanking.)

The subcarrier is generated by crystal oscillator Q38 and Q39, and is buffered by Q40. The oscillator runs at four times subcarrier frequency to provide four clock phases at subcarrier frequency at 90° increments. The four phases are generated in the Johnson counter U37. Two of these phases are used for the U and V subcarriers. Any one of the four available phases may be selected by U36 for the input of one-shot U35. The one-shot is used as a variable phase shifter to allow fine adjustment of the system subcarrier phase. The output of U35 pin #4 is connected to the second section of U35 which is used to re-establish a duty cycle of about 50%.

The output of U35 is then passed to one input of phase comparator U25. The other input is provided by burst gate switch Q29 and Q28, which gates the burst from the chroma signal provided by burst amplifier Q27 and Q30. The output of U25 is amplified and sampled by U27 to produce a phase error signal across C92. This error signal is filtered and amplified by amplifier U38 and applied to the varicap CR6 to correct the oscillator frequency. The burst sample pulses for U27 (and U26 in PAL) are provided by one-shot U28. In the absence of reference video and during the vertical interval, the sample pulses are inhibited by signals on U28 clear inputs. (In PAL systems the output of U26 is amplified by Q32 to produce negative-going pulses on every alternative line to synchronize the PAL switching.)

SECTION 4

Troubleshooting

4.1 INTRODUCTION

This section provides maintenance personnel with systematic procedures to isolate the cause of system failures down to specific areas (i.e. a printed circuit board or particular servicable component.)

Many component failures require specialized test fixtures and equipment that are not available at standard test facilities. Therefore, these test procedures are based on the use of standard test equipment (outlined below) with the VP-2 operating as a test fixture.

These procedures assume that the technician is thoroughly familiar with test procedures and equipment in general, and with the VP-2 functional theory described in Sections 2 and 3 of this manual.

Once a problem has been isolated to a printed-circuit board, the faulty board can be removed and shipped to CHYRON® for repair or replacement. Paragraph 4.9 provides detailed removal, packing, and shipping instructions. In the event that the problem is caused by a faulty servicable component, follow the instructions in the appropriate paragraph.

The following test equipment is required to perform these troubleshooting procedures:

- Digital Multimeter
- Dual Trace Oscilloscope (100MHz or above)
(TEKTRONIX® 2235 or equivalent)
- Sync Generator

NTSC: TEKTRONIX® Model 1410 or equivalent
PAL : TEKTRONIX® Model 1411 or equivalent
PAL-M: TEKTRONIX® Model 1412 or equivalent
- Vectorscope

NTSC: TEKTRONIX® Model 520A or equivalent
PAL : TEKTRONIX® Model 521A or equivalent
PAL-M: TEKTRONIX® Model 522A or equivalent

4.2 QUICK TROUBLESHOOTING GUIDE

Use this guide to determine/isolate general problems into categories of symptoms. To use, find the particular problem in the "SYMPTOM" column, and take the appropriate corrective action. If more detailed troubleshooting is necessary, the "CORRECTIVE ACTION" column will refer to a subsection that will provide additional information.

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
No power	No power at receptacle	Check for proper voltage and contact at receptacle.
	Blown fuse	Replace fuse. Refer to Paragraph 4.3.
	Short-circuit in unit.	Refer to Paragraph 4.3.
	Faulty power supply	Refer to Paragraph 4.3.
Red Screen at Power-up	Unseated Dual Processor Board, unseated I/O Board.	Reseat Dual Processor Board. Reseat I/O Board.
	Dual Processor Board failure	Refer to Paragraph 4.4.
	Font Memory Board failure	Refer to Paragraph 4.5.
	Main Logic Board failure	Refer to Paragraph 4.6.
Horizontal jagged lines on screen. Screen anomalies. Blank screen. Random patterns.	Lack of timing for bus arbitration circuit.	Re-seat 34-wire ribbon cable from J1 on the Main Logic Board to J12 on the Sync Gen/Encoder Board.
Character tearing after normal power-up. (<u>NOT</u> a video problem).	Shared RAM Failure	Verify proper video operation with vectorscope/waveform monitor. Refer to Paragraph 4.4 for more information on shared RAM anomalies.

SYMPTOM	PROBABLE CAUSE	CORRECTIVE ACTION
Red screen. Error message, "PAGE A EVEN FAIL" "PAGE A ODD FAIL" "PAGE B EVEN FAIL" "PAGE B ODD FAIL"	VRAM failure, Main Logic Board.	Refer to Paragraph 4.6, Main Logic Board Troubleshooting.
Red Screen. "DISK ERROR" message after normal power-up, before or during disk drive operation	Disk insertion error.	Re-insert disk into disk-drive.
	Bad disk.	Re-initialize disk. Replace disk. See Appendix.
	Drive-I/O board cable connection	Re-seat connectors. See Appendix.
	Faulty power-supply circuitry	Check to see if drive motor rotates (see paragraph 4.7.2). Check for 12vdc supply voltage at disk drive, and at power supply. Refer to Paragraph 4.3 for more information.
	Bad floppy-disk controller, bad disk drive	Refer to Paragraph 4.7.2 for more information.

4.3 POWER SUPPLY DIAGNOSIS PROCEDURE

CAUTION!!!

Power-supply circuitry contains hazardous voltages. Prevent electrical shock hazards by disconnecting the AC power source while working within the unit, or by avoiding the AC power connections while servicing the unit under power.

In this troubleshooting procedure, refer to Figure 4-1, Power Supply Top View.

Step 1: Using a voltmeter, check the AC receptacle for the proper voltage.

Step 2: Check the continuity of the fuse using an ohmmeter. If the fuse is blown, replace it with a 3-amp cartridge fuse.

NOTE: If the fuse blows repeatedly, the power supply itself is faulty and must be replaced. The power supply has a cut-out feature that prevents the fuse from blowing when a short-circuit occurs on one of the circuit boards within the unit. Refer to Paragraph 4.9 for removal/replacement procedures.

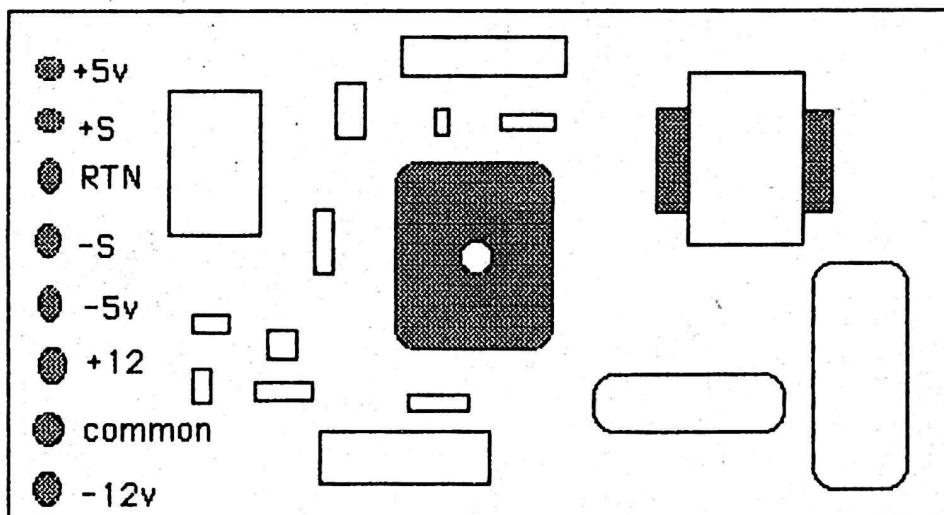


Figure 4-1. Power Supply, Top View

Step 3: Refer to Figure 4-1. Check the power supply for +5v DC at the terminal marked "+5" with a voltmeter. If +5v DC is present, proceed to Step 5. If +5v DC is NOT present, remove connections to the power supply one at a time, to isolate a possible short to one of the internal circuit boards. Each of the following subassemblies have a separate power connector, which is directly connected to the power supply. Disconnect the subassemblies in the following order while monitoring the +5 terminal in order to isolate the short-circuit.

A. Disk Drive

B. I/O P. C. Board

C. Main Logic P. C. Board

D. Sync Gen/Encoder P. C. Board

+5v should be restored to "+5" terminal when the short is removed. Refer to the appropriate section to further troubleshoot the specific board failure.

Step 4. If +5v is not restored after removing all the loads, place a simulated load on the power supply. Connect a 250-Ohm, 5-Watt (or similar) resistor between the +5 terminal and ground. If power still does not return, the power supply is faulty and must be replaced. Refer to Paragraph 4.9.7 for replacement procedure.

NOTE: The power supply will not produce ± 12 volts unless the ± 5 volt circuitry is functioning properly.

Step 5: If +5 volts DC is present at the "+5" terminal, check for +12 volts DC at the "+12" terminal on the power supply (refer to Figure 4-1). If +12 is not present, monitor the terminal and disconnect the power connectors from the boards in the order outlined in Step 3. The +12 volt level will return when a short is removed. If the short is isolated to a particular P. C. board, refer to the appropriate section to troubleshoot further.

Step 6: If the +12v level is not restored by removing all power connectors, the power supply is faulty and must be replaced. Refer to Paragraph 4.9 for replacement procedures.

4.4 DUAL PROCESSOR P. C. BOARD DIAGNOSTIC PROCEDURE

Refer to the Dual Processing Board Schematics (Figure 7-1) throughout this paragraph for further information.

Locate the LEDs DS1, DS2, and DS3 on the right side of the Dual Processor Board. These lights provide useful information as to the operation of the board.

Each LED demonstrates a particular function of the board. DS1 (green) acts as an 8088 CPU "run" light. DS2 (red) acts as an 80186 CPU "run" light. DS3 is a two-color LED that displays either red or green, or a combination of both colors.

4.4.1 Initial Troubleshooting

1. Inspect the Dual Processor Board for loose connectors. Inspect for bent or broken IC pins.
2. Inspect the 8088 CPU. Check for broken or bent pins.
3. Make sure that the 80186 CPU is properly seated into its socket. Refer to Figure 4-2 and the following procedure to remove and re-seat the CPU.

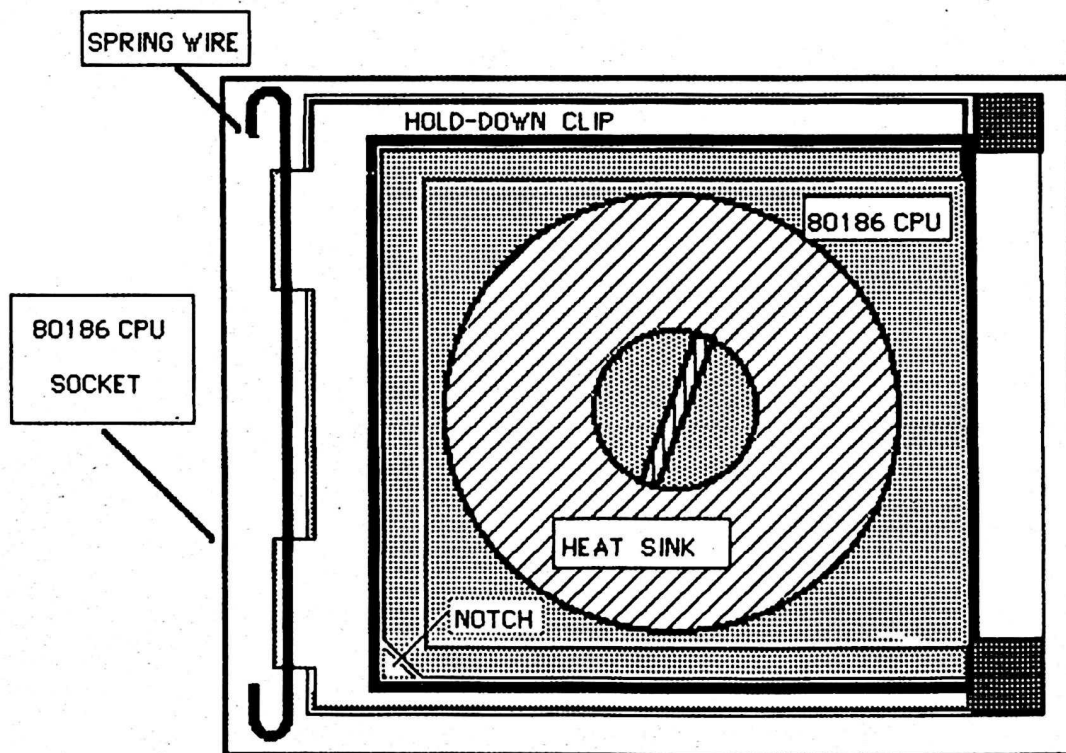


Figure 4-2. 80186 CPU Socket

4.4.1.1 80186 CPU Removal/Re-Seating

- (1) Grasp the heat sink firmly by the edges and turn counterclockwise to remove it.
- (2) Using a small, flat-blade screwdriver, pry the spring wire away from the two tabs on the hold-down clip. Refer to 80186 Socket Assembly Drawing, Figure 4-3.
- (3) Lift the hold-down clip away from the CPU chip. Note the orientation of the CPU.
- (4) Grasp the heat sink center post and lift straight up.
- (5) Clean the contacts of the socket and CPU chip with a lint-free cloth and alcohol.
- (6) Replace the CPU chip in the socket. Be sure to orient the chip properly by observing the notch on one corner.
- (7) Replace the hold-down clip with the open side away from the socket's spring wire.
- (8) Press down on the hold-down clip and pry the socket's spring wire over the hold-down clip's two tabs.
- (9) Re-thread the heat sink onto the heat sink post.

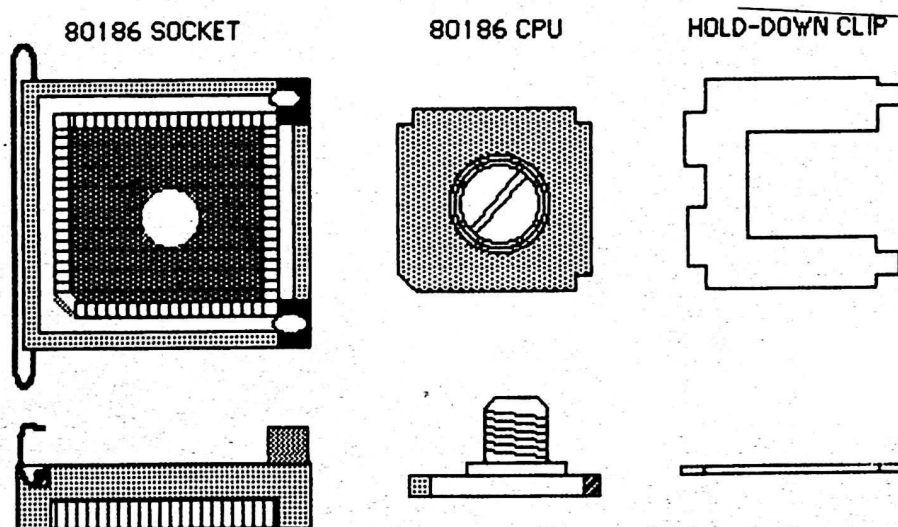


Figure 4-3. 80186 Assembly Drawing

4.4.2 Troubleshooting from Run-Light Situations

The three LED run-lights (DS1, DS2, and DS3) provide status information on the 8088 and 80186 CPUs. In this subsection, various run-light illumination patterns will be examined in detail.

To use this section, examine the run-lights in the unit under test. Locate the illumination pattern in this section, and follow the troubleshooting procedure provided.

The following illumination patterns are detailed in this subsection:

- 8088 Run-Light (GREEN) is ON, 80186 Run-Light (RED) is OFF
- 8088 Run-Light is OFF, 80186 Run-Light is OFF

4.4.2.1 8088 Run-Light On, 80186 Run-Light Off

Step 1: Power down the VP-2.

Step 2: (a) Disconnect 60-wire ribbon cable from connector P1.

(b) Power on the VP-2. If the 80186 run-light does not go on, proceed to step 3.

Step 3: (a) Using the oscilloscope, check for an 8.0 MHz square wave at P3, pin #6 (see Figure 4-4, Waveform A). If the proper signal is present, go on to Step 4.

(b) Inspect Crystal Y1 for cold solder joints, etc. If necessary, replace Y1 or ship board to CHYRON® for replacement.

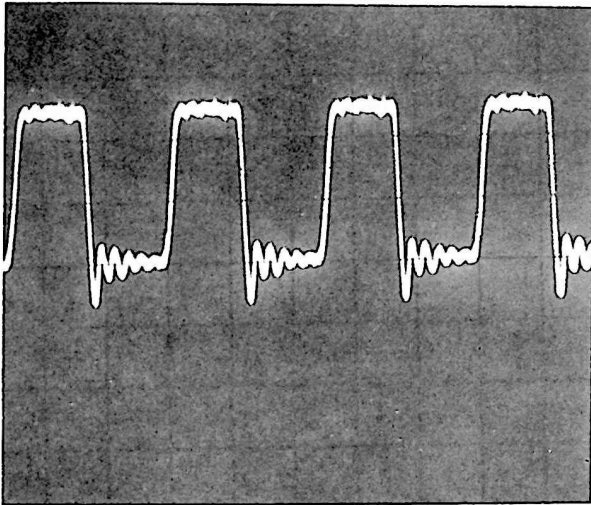
Step 4: (a) Using the oscilloscope, check U35 pin 11 for a mostly high waveform with low-going pulses. Check U35 pin 12 for the same waveform. If the waveform is present, go on to Step 5. If the waveform is not present, continue with Step 4.

(b) Inspect chips U5, U6, U7, and U8. Check for bent or broken pins. If necessary, re-seat the chips. If the proper waveform appears at U35 pin 12, go on to step 5.

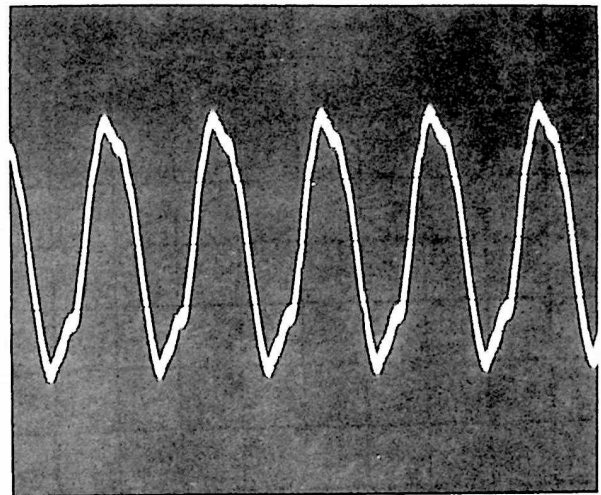
(c) Inspect 510-ohm, 1/4 Watt resistor R11 for shorts or breakage. Replace if necessary.

Step 5: (d) Using the oscilloscope, check U35 pin 13 for a mostly high signal, with an occasional low-going pulse. If this signal is present, go on to Step 6.

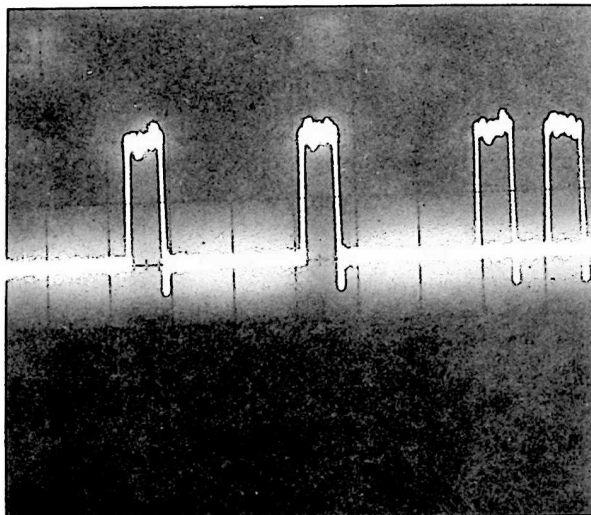
- (b) Place the oscilloscope probe at U38 pin 11. Check for a 23 MHz clock signal (see Figure 4-4, Waveform B). If the clock signal is present, go to step 6.
 - (c) Place the probe at U38 pin 3 and check for the same 23 MHz clock signal. If the clock signal is present on U38 pin 3 but not on U38 pin 11, either replace U38 or ship the board to CHYRON® for replacement.
 - (d) Place the probe at P4 pin 8. Check for the 23-MHz clock signal. If the proper clock signal is not present, refer to Paragraph 4.6, Main Logic Board Troubleshooting.
- Step 6:
- (a) Place the oscilloscope probe on U36 pin 6. If the pin is mostly high, with an occasional low-going pulse, go on to Step 7.
 - (b) If pin 6 is "stuck" low, place the probe at P2 pin 23. If this pin is mostly high, with an occasional low-going pulse, check the seating of U17 and U37. If P2 pin 23 is "stuck" low, see Paragraph 4.6, Main Logic Board Troubleshooting.
- Step 7:
- (a) Using the oscilloscope probe, check U2 pin 11 for the waveform shown in Figure 4-4, Waveform C. If the waveform is present, go on to step 8.
 - (b) If the waveform is not present, the board should be replaced. See Paragraph 4.9.
- Step 8:
- (a) Place the oscilloscope probe at U9 pin 20, and check for the waveform shown in Figure 4-4, Waveform D. If the waveform is present, go on to step 9.
 - (b) Place the probe on U35 pin 8. If the above waveform is present, check the seating of U9 and U35, and check that jumper J3 from C to B is intact. Check for cold solder joints.
 - (c) If the waveform shown in Figure 4-4 Waveform D does not appear at U9 pin 20, the board should be shipped to CHYRON® for repair. See Paragraph 4.9 for board removal instructions.



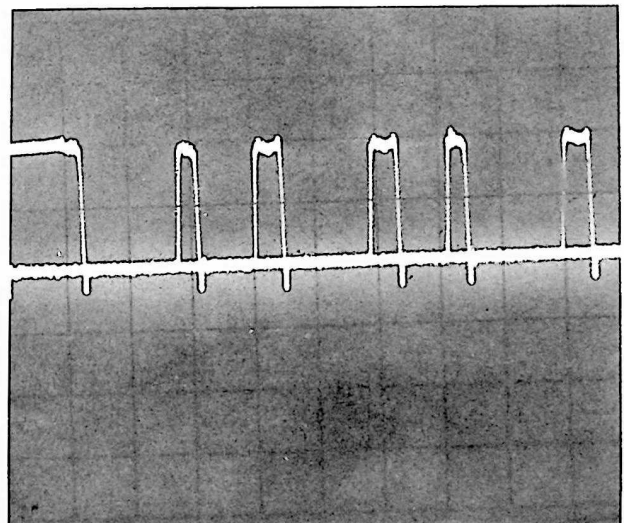
Waveform A
8-MHz clock @ P3 pin 6
X=0.05 μ S/div Y=0.2V/div



Waveform B
ARBCLK @ P4 pin 8
X=0.05 μ S/div Y=0.1V/div



Waveform C
@ U2 pin 11
X=0.2 μ S/div Y=0.2V/div



Waveform D
@ U9 pin 20
X=0.5 μ S/div Y=0.2V/div

Figure 4-4. Dual Processor Board Waveforms

- Step 9: (a) Place the oscilloscope probe on U30 pin 12 with the oscilloscope negative-edge triggered.
- (b) Look for a 400-nanosecond pulse, each time the power switch is turned on.
- (c) If the pulse is not present, inspect U30, R3, and C5. Look for short-circuits, broken leads, or cold solder joints. If these components are functional, refer to Paragraph 4.6, Main Logic Board Troubleshooting.

4.4.2.2 8088 Run-Light Off, 80186 Run-Light Off

- Step 1: (a) Remove the power connector from the lower left corner of the Dual Processor Board near the 80186 CPU.
- (b) Using the digital multimeter, check the connector for +5 volts. If +5 volts is not present, see Paragraph 4.3, Power Supply Troubleshooting.
- (c) Replace the power connector, making sure that the pins are making good contact.
- Step 2: (a) Using the oscilloscope, check P4 pin 8 for a 23 MHz arbitration clock signal. If the signal is not present, make sure board is properly seated and check pin 8 again. If the 23 MHz signal still is not present, refer to Paragraph 4.6, Main Logic Board Troubleshooting.
- (b) Check U38, pins 1 and 13 for +5 volts. If +5 volts is not present, inspect R10 for damage or for cold solder joints. If +5 volts is still not present, the board is faulty and must be shipped to CHYRON for repair. Refer to Paragraph 4.9 for board removal instructions.
- (c) Using the oscilloscope, check U38 pin 11 for the 23 MHz clock signal. If the signal is not present, the board is faulty and must be replaced. Refer to Paragraph 4.9.
- (d) Check U25 pin 13 for the 23 MHz clock signal. If the signal is not present, refer to Paragraph 4.9.
- (e) Check U25 pin 12 for the 23 MHz clock signal. Then, check U38 pin 3 for the same signal. If the signal is not present at either of these places, the board is faulty and must be replaced. Refer to Paragraph 4.9.

NOTE: Should you encounter a difficulty not covered by these procedures, contact your CHYRON distributor or the CHYRON Customer Service Department for further assistance. Please do not return any material to us without a Material Return Authorization (MRA).

4.4.3 General CPU Troubleshooting Hints.

Using an oscilloscope, the technician can detect many conditions involving address or data lines within the VP-2 unit. Since the 8088 and 80186 CPUs have multiplexed address/data lines, they each must produce a signal called ALE (Address Latch Enable) which is used to determine when lines carry address information and when they carry data.

The following procedure will help locate physical phenomena that may affect the address/data, such as grounded or crossed lines.

4.4.3.1 80186 CPU Address/Data Line Troubleshooting

Step 1: (a) Synchronize the oscilloscope to the falling edge of ALE, which is present on U1 pin 11.

(b) Refer to Section 7, Figure 7-1 to locate the address/data lines. Check each of the address lines A_0-A_{15} with the oscilloscope. At the falling edge of ALE, each of the address lines must be either a logical "high" or "low". If all lines meet this condition, go on to Step 2.

(c) Refer to the Dual Processor P. C. Board Schematic Diagram in Section 7. Trace each faulty address line from point to point on the P. C. board. Look for foreign material that may be causing lines to cross. Check the address latch chip that carries the address line (A_0-A_7 is carried by U3, A_8-A_{15} is carried by U2). If necessary, replace the address-latch chips.

Step 2: (a) Synchronize the oscilloscope to the rising edge of the RD86 signal (present on U5 pin 22).

(b) Locate each of the data lines D_0-D_{15} on the Dual Processor Board Schematic Diagram in Section 7, Figure 7-1. Check each data line for either a "high" or "low" level. If all lines meet this conditions, go on to the 8088 CPU Address/Data Line Troubleshooting paragraph.

(c) Refer to the schematic diagram. Trace each data line from point to point on the P. C. board. Look for foreign material that may be causing any voltage level besides a "high" or "low". Check the seating of all socketed chips that access the bad data line(s).

4.4.3.2 8088 CPU Address/Data Line Troubleshooting

Step 1: (a) Synchronize the oscilloscope to the falling edge of ALE88, present on U19 pin 11.

- (b) Locate each of the address lines on the Dual Processor board schematic diagram (AD₀-AD₇ thru A₁₉ are all address lines). Check each data line for either a "high" or a "low" signal. If all lines meet this condition, return to the Quick Troubleshooting Guide, Paragraph 4.2.
- (c) Refer to the schematic diagram. Trace each faulty address line from point to point. Look for any foreign material that could cause a short or crossed lines. Inspect the address-latch chips U19 on the Dual Processor board, and U92 on the Main Logic P. C. Board. Replace the faulty chip(s) if necessary.

- Step 2:
- (a) Synchronize the oscilloscope to the rising edge of the WR88 signal (present on U39 pin 8).
 - (b) Refer to the schematic diagram. Check the data lines AD₀-AD₇ for either a "high" or "low" level. If all data lines meet these conditions, refer to the Quick Troubleshooting Guide, Paragraph 4.2.
 - (c) Trace any data line that does not show either a "high" or "low" level from point to point on the P. C. board. Look for any foreign material that could cause a short circuit or crossed data lines.

4.4.4 Troubleshooting from Error Messages

ERROR MESSAGE	CORRECTIVE ACTION
"TEST 186 FAILURE"	Replace local IRAM chips U5, U6.
"SHARED RAM FAILURE"	Replace static RAM chips U22 and U23.

NOTE: Should you encounter a difficulty not covered in these procedures, contact your CHYRON distributor or the CHYRON customer service department for further assistance. Please do not return any material without a Material Return Authorization (MRA).

4.5 FONT MEMORY P. C. BOARD TROUBLESHOOTING

This troubleshooting procedure verifies Font Memory operation, and isolates and/or corrects difficulties. For further information, refer to the Font Memory P. C. Board Schematics, Figure 7-2.

Step 1: (a) Power down the VP-2. Remove the top cover.

(b) Remove the 60-wire ribbon cable from P1 on the Dual Processor P. C. Board.

(c) Power on the VP-2. If the unit still responds with a red screen, the Dual Processor board is causing the failure. See Paragraph 4.4. If the unit responds with a blue screen and an error message "NO FONT IN SOCKET 1", proceed to Step 2.

Step 2: (a) Reconnect the 60-wire ribbon cable to P1 on the Dual Processor Board.

(b) Disconnect the other end of the 60-wire ribbon cable from J1 of the font board.

(c) Power on the unit. If the unit responds with a red screen, the 60-wire ribbon cable is faulty and must be replaced.

Step 3: (a) Remove the power connector lug from the upper left corner of the font memory board. Using the digital multimeter, check for +5 volts. If +5 volts is not present, refer to Paragraph 4.3, Power Supply Troubleshooting.

(b) Power down the VP-2. Reconnect the power lug. Reconnect the 60-wire ribbon connector to J1 of the font board. Remove all fonts from their sockets.

(c) Power on the unit. If the unit responds with a red screen, the Font Memory P. C. board is faulty and must be replaced. Refer to Paragraph 4.9. If the unit responds with a blue screen and an error message "NO FONT IN SOCKET 1", proceed to Step 4.

Step 4: (a) Power down the unit. Clean all font chip pins with alcohol and a lint-free cloth.

(b) Insert one font chip into the unit's font socket F1. Open and close the socket several times to remove any corrosion.

(c) Power up the VP-2. If the unit powers up normally, power down the unit, remove the "good" font chip, and repeat Step 4 (b) with each of the remaining font chips. Any font chip that causes the unit to respond with a red screen is faulty and should be replaced.

4.6 MAIN LOGIC P.C. BOARD TROUBLESHOOTING

This subsection isolates and/or corrects faults on the Main Logic board. During the troubleshooting procedures, refer to the Main Logic P. C. Board Schematics, Figure 7-3.

4.6.1 Interrupt Controller Failures

- (a) On the Dual Processor P. C. Board, look for the 60-Hz Vertical Blanking signal on the 8088 CPU, U14 pin 18. See Figure 4-5, Waveform A for the proper waveform. If the waveform is present, go on to Step 2.
- (b) Power down the VP-2. Remove the Dual Processor board using the procedure detailed in Paragraph 4.9.
- (c) On the Main Logic P. C. Board, inspect the interrupt jumper matrix (J24, J25) for loose or broken wires, or for cold solder joints. See Figure 4-5 for the proper arrangement of the jumper wires.

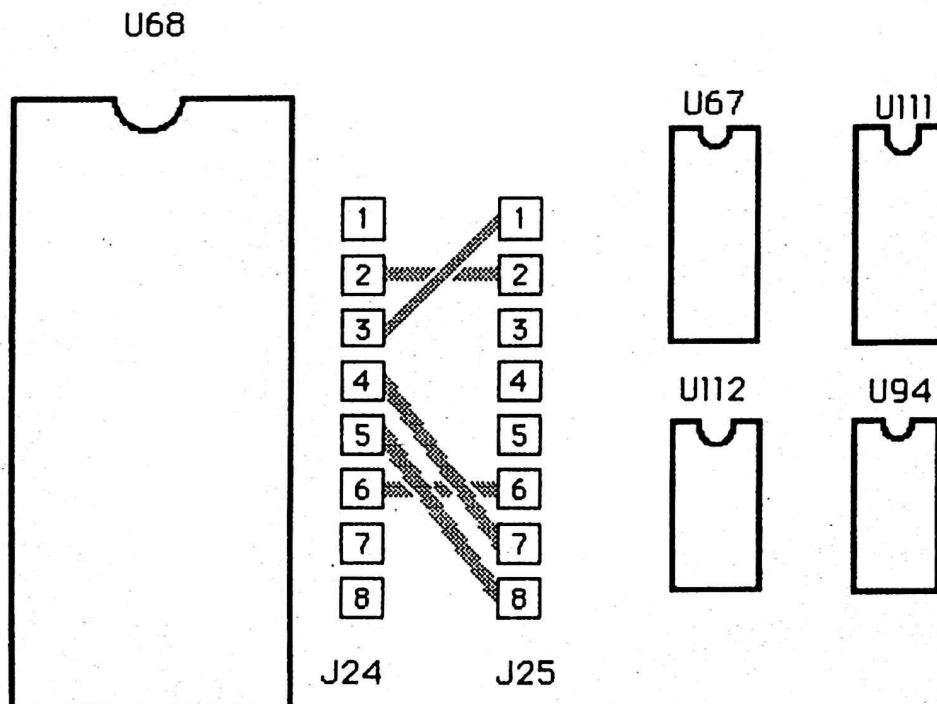


Figure 4-5. Interrupt Controller Jumpers

- (d) Using the oscilloscope, check U19 pin 3 for the 60-Hz vertical blanking signal. If the proper waveform is present, then check for continuity between U68 pin 21 and U19 pin 3.
- (e) Check U19 pin 4 for the 60-Hz vertical blanking signal.
If the proper waveform is not present, refer to Paragraph 4.8, Sync Gen/Encoder Board Troubleshooting.

4.6.2 CPU/Arbitration Clock Signal Troubleshooting

The 8088 CPU clock signal and the shared RAM arbitration clock signal are both derivatives of a 23.040 crystal. The crystal oscillator circuitry consists of U79, crystal Y1, diode CR1, capacitor C2, and resistor R1. Since the crystal oscillator will operate independently of CPU control, the dual processor board can be removed from the unit to expose the portion of the main logic board that carries the oscillator circuitry.

Step 1: Remove the Dual Processor board using the procedure outlined in Paragraph 4.9.2.

- Step 2:
- (a) Visually inspect the crystal oscillator circuitry (located near the front edge of the Main Logic Board). Check for loose or broken leads on the crystal and other components. Make sure oscillator chip U79 is seated properly in its socket.
 - (b) Power up the unit. Using the oscilloscope, check pin 19 of the 40-pin DIP connector of the Dual Processor board for an 8 MHz clock signal. If this signal is present, inspect the underside of the Dual Processor board for bent or missing pins. Check that the DIP connector is making good contact.
 - (c) Using the oscilloscope, check U79 pin 8 for an 8 MHz clock signal. If this signal is present, check for continuity between pin 19 of the DIP connector and U79 pin 8.
 - (d) If the 8 MHz clock signal is not present at U79 pin 8, inspect crystal Y1. Tap the crystal gently to determine if the crystal is physically damaged. If necessary, replace crystal Y1.
 - (e) If the 8 MHz clock signal is still not present, replace U79.

4.6.3 Troubleshooting from Error Messages

ERROR MESSAGE

CORRECTIVE ACTION

"SCRATCHPAD RAM FAILURE"

Inspect U61, U62, and U89. Make sure the devices are properly installed in their sockets. Check for bent pins.

Replace U61, U62, and U89 or replace Main Logic Board. See Paragraph 4.9.

"PAGE A EVEN FAIL"

Replace VRAM chips U20-U27.

"PAGE A ODD FAIL"

Replace VRAM chips U29-U36.

"PAGE B EVEN FAIL"

Replace VRAM chips U1-U8

"PAGE B ODD FAIL"

Replace VRAM chips U10-U17

"BUFFER SWITCH ERROR"

Inspect devices associated with the page-switching logic, especially U93, U58, U59, and U80.

If the corrective actions taken do not remedy the difficulty, contact the CHYRON® customer service department for further assistance. Refer to Paragraph 4.9 and Paragraph 4.10.

4.7 I/O P. C. BOARD TROUBLESHOOTING

Refer to the I/O P. C. Board Schematics (Figure 7-4) during these troubleshooting procedures.

This paragraph addresses the four sections of the I/O board individually. These sections are:

- Edit Channel
- Floppy Disk Controller
- Keyboard Interface
- Alarm Interface

4.7.1 Edit Channel Troubleshooting

Problems on the Edit Channel are identifiable simply by checking the other outputs of the VP-2. For example, if the Edit Out channel is not operating properly, and the cause of the problem is the Edit Channel, the other VP-2 outputs (Program "A" Out, Program "B" Out) will not be affected.

This troubleshooting procedure assumes that the technician has checked the other video outputs and has determined that the observed problem is being caused by the Edit Channel circuitry. The step-by-step procedure will identify and correct most Edit Channel difficulties.

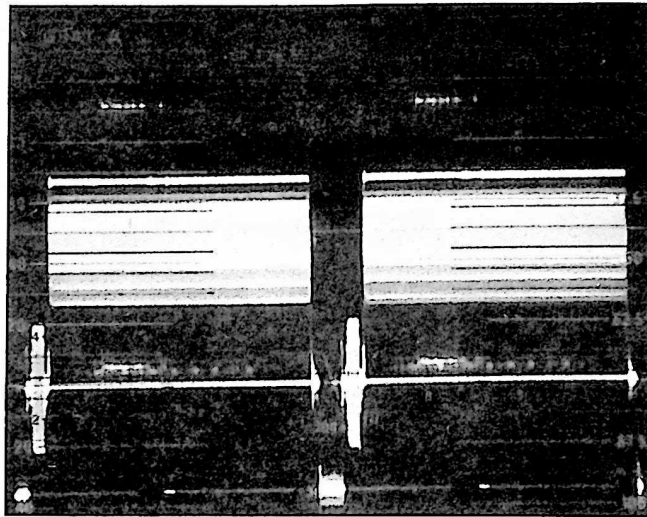
Step 1: (a) Using the oscilloscope, check J7 pin 2 on the Sync Gen/Encoder board for a signal similar to the NTSC composite video signal shown in Figure 4-6, Waveform A. If this signal is not present, refer to Paragraph 4.8, Sync Gen/Encoder Board Troubleshooting.

(b) Make sure all three connectors are properly seated at J4 on the I/O board. Inspect cables for visible damage. Replace cable(s) if necessary.

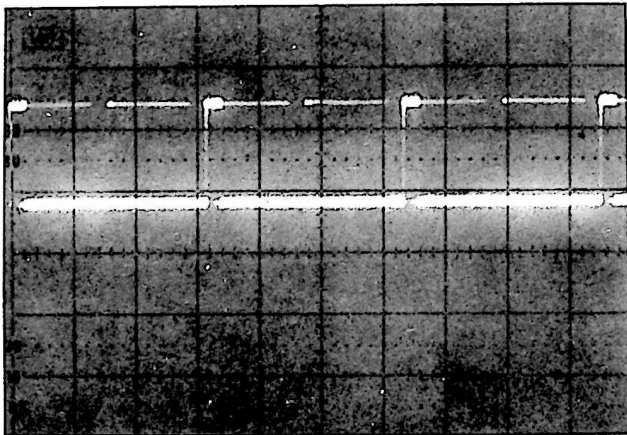
Step 2: (a) Using the oscilloscope, check U4 pin 34 for the Sync Reset signal (see Figure 4-6, Waveform B). If the Sync Reset signal is present, go on to Step #2.

- (b) If the Sync Reset signal is not present at U4 pin 34, inspect resistors R18 and D2 (shown as R1 in later board revisions) for damage and/or cold solder joints.
- (c) Check U26 pin 6 for the same Sync Reset signal. (NOTE: Since this circuitry acts as a sync level-shifter, the voltage level of the signal will differ from place to place. However, the waveform will be similar in each location.) If the signal is present, re-seat U26 and check the P. C. board for cold solder joints.
- (d) Check U26 pin 5 for the Sync Reset signal. If the signal is present, re-seat U26 and check for cold solder joints. If necessary, replace U26.
- (e) Locate J11 on the Sync Gen/Encoder P. C. Board (J11 is the origin of the Sync Reset signal. A cable connects J4 on the I/O board and J11 on the Sync Gen board). Remove the connector from J11. Check J11 pin 2 for the Sync Reset signal. If the proper signal is not present, then the fault is on the Sync Gen/Encoder P. C. Board. Refer to Paragraph 4.8. If the signal is present, check the cable connections between J4 on the I/O board and J11 on the Sync Gen Board. Also, check continuity between J4 pin 8 and U26 pin 5. Look for shorts, solder bridges, or cold solder joints.

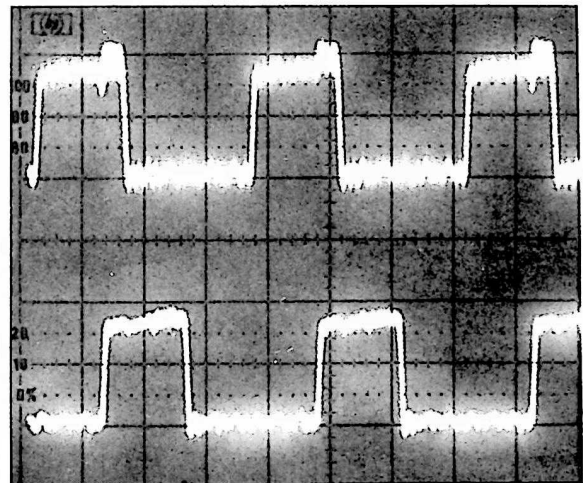
- Step 2:
- (a) Using the oscilloscope, check U4 pins 39 and 40 for an 11.4 MHz clock signal. If this clock signal is present, go on to Step 3.
 - (b) Check U15, pins 2 and 12 for the 11.4 MHz clock signal. If the signal is present, check for continuity between U15 and U4.
 - (c) Check U15 pin 1 for the 11.4 MHz signal. If the signal is present, inspect the chip for damage or cold solder joints. If necessary, replace the chip.
 - (d) Check pin 14 of U14 for the 11.4 MHz clock signal. If the clock signal is present, check continuity between pin 14 of U14 and pin 1 of U15.
 - (e) Check pin 2 of U14 for a 28 MHz clock signal. If this signal is present, replace U14.
 - (f) If the 28 MHz signal is not present, check P1 pin 6 (SBX Bus) for the 28 MHz signal. If the 28 MHz signal is not present, refer to Paragraph 4.6, Main Logic P. C. Board Troubleshooting.



Composite Video Signal
Waveform A



Sync Reset Signal
@ U4 pin 34
X=0.02ms/div, Y=0.5 v/div



RAS (upper), CAS (lower)
@ U4 pins 1, 2
X=0.1us/div, Y=0.2 v/div

Figure 4-6. I/O Board Waveforms

- (c) If both of the above signals are present and edit channel anomalies continue, inspect the VRAM chips U5-U12. Be sure the chips are properly seated, and have no bent or broken pins. If this does not correct the problem, remove the board (see Paragraph 4.9 for instructions) and inspect its foil side for shorts or cold solder joints. Inspect the SBX bus connector for damage. Replace the board, and make sure it is seated properly. If the edit channel still does not operate properly the board requires factory repair. Refer to Paragraphs 4.9 and 4.10 for removal and shipping instructions.

4.7.2 Floppy Disk Controller Troubleshooting

The floppy-disk controller is based on the 8272 floppy-disk controller chip. The controller circuitry generates its own 8 MHz clock signal, which is divided into various other clock rates as required. The troubleshooting procedure aims to isolate floppy-disk problems to the controller circuitry, or to the disk-drive unit itself. As with the Edit Channel circuitry, disk drive problems are difficult to describe accurately. However, the troubleshooting procedures will isolate most operational difficulties.

- Step 1:
- (a) Inspect the disk drive. Check to see that all connectors are securely fastened.
 - (b) Open the VP-2 front panel. Place an initialized disk into the drive, power up the unit, and call up a disk directory. Look at the underside of the disk drive unit while the disk drive is operating. If the drive "platter" spins when the directory is requested, go on to Step 2.
 - (c) If the drive "platter" does not spin when it should, check the power connector. Remove the connector, and check for the proper voltages (the disk drive unit's power connector carries +12v, +5v, and two grounds).
 - (d) Reconnect the power cable to the disk drive. Either call up a disk directory or create a repeating auto-display file (see the VP-2 Operator Manual). Using the oscilloscope, check U25 pin 7 for a mostly low signal with high-going pulses when the drive should be operating. If these signals are not present, the disk drive may be faulty. See Paragraph 4.9 for drive removal instructions.
- Step 2:
- (a) Using the oscilloscope, check U28 pin 19 for a 4 MHz clock signal. If this signal is present, go on to Step 2.
 - (b) Check U21 pin 5 for the 4 MHz clock signal. If this signal is present, check for continuity between U28 pin 19 and U21 pin 5. Inspect each chip. Check for short circuits. Be sure each chip is properly seated.

- (c) Check U21 pin 1 for an 8 MHz clock signal. If this signal is present, inspect U21. Check seating, and look for bent/broken leads. If necessary, replace U21.
- (d) Check U22 pin 3, U20 pin 1, and U24 pin 9 for the 8 MHz clock signal. If the 8 MHz clock signal is not present, inspect each chip for proper seating. Check also for bent or broken pins. If the signal still is not present, the board requires factory repair. See Paragraph 4.9 for board removal instructions.

Step 3: (a) Power down the VP-2. Place one probe of the oscilloscope on U15 pin 10.

- (b) Insert an initialized disk into the disk drive. Power up the unit, and call up a disk directory. The oscilloscope should show a mostly low signal, with high-going pulses. If this signal is not present, place the probe on U15 pin 11. Call up the disk directory again. If the signal is present, inspect U15 for damage or short-circuits.
- (c) Place the oscilloscope probe on U22 pin 7. Call up the disk directory. Look for a mostly high signal with low-going pulses. If this signal is present, check for continuity between U22 pin 7 and U15 pin 11.
- (d) Place the oscilloscope probe on U22 pin 1. Call up the disk directory. Look for a mostly high signal with low-going pulses. If this signal is present, check U22 for proper seating. Inspect the chip for bent or broken pins. If necessary, replace the chip.
- (e) Place the oscilloscope probe on U27 pin 4. Call up a disk directory. Look for the same signal (RAWDAT, mostly high with low-going pulses). If the signal is present, check for continuity between U27 pin 4 and U22 pin 1. Look for short circuits, etc.
- (f) Place the oscilloscope probe on U27 pin 3. Call up the disk directory. Look for an inverted RAWDAT signal (mostly low with high-going pulses). If this signal is not present, inspect ribbon-cable connector J5. Look for damage, and check for proper connector seating. Refer to Appendix A for more information about the floppy-disk drive.

Step 4: If all signals appear where and how they are supposed to, and the floppy disk controller continues to retrieve bad data from the disk, then the data separator (U22) is suspect. The data separator is a specialized PROM device that is susceptible to static discharges. A static discharge could alter some of the data stored in the PROM, causing it to fail in an unpredictable manner. Replace the data separator chip, or ship the I/O board to CHYRON® for repair. See Paragraph 4.9 for board removal procedures.

4.7.3 Keyboard Interface Troubleshooting

The keyboard interface on the I/O board converts serial data from the Keytronics keyboard (See Keytronics Keyboard Schematics in Section 7). The circuitry consists of serial-to-parallel converter U32, flip-flop U33, line receiver/RS422 driver U13, and inverting buffer U16. Follow this brief troubleshooting procedure if there is any doubt of the keyboard interface's operation. This procedure will verify keyboard interface operation and isolate any faults.

- Step 1: (a) Place an oscilloscope probe on U33 pin 5. Press any key on the keyboard and hold it down. The oscilloscope should show a mostly low signal with high-going pulses. If these signals are present, then the keyboard interface is generating the proper interrupt pulses. If this signal is not present, make sure the keyboard cable is connected to the rear panel of the unit. Also, inspect J2 on the I/O board, and make sure the connector is properly seated.
- (b) Place the oscilloscope probe on U33 pin 2. Press any key on the keyboard, and hold it down. Check for a mostly low signal with high-going pulses. Check for the same signal at U32 pin 8. If this signal is present at only one of these locations, check for short-circuits, etc.
- (c) If the above signal is not present at either location, inspect both chips and check for damage.
- (d) Place the probe at U16 pin 6. Press and hold any key on the keyboard. The oscilloscope should show a mostly low signal with high-going pulses. If this signal is not present, place the probe on U16 pin 5. Check for a mostly high signal with low going pulses. If this signal is present, inspect U16 for damage. Replace if necessary.

- (e) Place the oscilloscope probe on U13 pin 13. Press and hold any key on the keyboard. Check for a mostly high signal with low-going pulses. If this signal is present, check for continuity between U13 pin 13 and U16 pin 5. If this signal is not present, check U13 pin 14 for the same signal. If this signal is present, inspect U13 for damage, bent/broken pins, or cold solder joints. If necessary, replace U13.
- (f) Place the oscilloscope probe on U32 pin 18. Press and hold any key on the keyboard. Check for a mostly high signal with low-going pulses. If this signal is present, go on to (i).
- (g) Place the oscilloscope probe on U13 pin 3. Press and hold any key on the keyboard. Check for a mostly high signal with low-going pulses. If this signal is present, check for continuity between U13 pin 3 and U32 pin 18.
- (h) Place the probe on U13 pin 2. Press and hold any key. Check for a mostly high signal with low-going pulses. If this signal is not present, inspect connector J2. Check for any damage.
- (i) If these troubleshooting procedures have not detected or isolated a problem within the keyboard interface system, please return to the Quick Troubleshooting Guide (Paragraph 4.2) for more information.

4.7.4 Alarm Interface Troubleshooting

The alarm interface is based on a one-shot chip (U30), and contains two discrete components and some simple decoding logic. Follow this procedure to correct any alarm abnormalities.

Step 1: Inspect the piezoelectric beeper (mounted on the chassis wall to the left of the I/O board, or on the I/O board, at the left rear corner) for any damage, and check for loose or frayed wires. On later revisions of the I/O board, the beeper is mounted on the I/O board. Inspect this mounting for damage.

Step 2: For units with the chassis-mounted beeper, check connector J1 for proper seating. Look for frayed wires and cold solder joints.

Step 3: Make sure the I/O board itself is properly seated.

4.8 SYNC GEN/ENCODER P. C. BOARD TROUBLESHOOTING

This troubleshooting procedure verifies Sync Gen/Encoder operation in the following modes:

- Stand Alone Black&White
- Stand Alone Color
- Genlocked Black&White
- Genlocked Color

4.8.1 Stand Alone B&W Verification

Step 1: Power off the VP-2.

Step 2: Disconnect the 40-wire ribbon cable between J4 on the Main Logic P. C. Board and J1 on the Sync Gen/Encoder P. C. Board.

Step 3: Connect a color video monitor to the Program "A" Out connector.

Step 4: Power up the VP-2. The video monitor should show a blank white screen. If a blank white screen does not appear, the board is faulty and must be repaired. Refer to Paragraph 4.9 for removal instructions.

4.8.2 Stand Alone Color Verification

Step 1: Do not reconnect the 40-wire ribbon cable between J4 on the Main Logic Board and J1 on the Sync Gen board. Connect the Program Out "B" Channel to one channel of the vectorscope.

Step 2: Check the vectorscope display for color burst. If burst is not present, the Sync Gen/Encoder board is faulty and must be repaired. See Paragraph 4.9.

4.8.3 Genlocked B&W Verification

Step 1: Do not reconnect the 40-wire ribbon cable. Hook a test video source from a sync generator to the Video In connector on the VP-2 back panel.

Step 2: Connect the Program Out "A" channel to one channel of a dual trace oscilloscope, and connect the Program Out "B" channel to the other channel of the oscilloscope.

Step 3: Display both channels on the oscilloscope screen. Check for alignment between each video signal's sync pulses. If the sync pulses are not aligned, the genlocking timing circuitry is not operational and the board must be repaired. Refer to Paragraph 4.9.

4.8.4 Genlocked Color Verification

Step 1: Do not reconnect the 40-wire ribbon cable. Connect the Program Out "A" channel of the VP-2 to Channel "A" of a vectorscope, and connect Program Out "B" to Channel "B" of the vectorscope.

Step 2: Connect a test color video signal to the VP-2 Video In connector.

Step 3: Set up the vectorscope as follows: Use Channel B with A-phase, and use Channel A as the Phase Reference.

Step 4: Display both channels of the vectorscope simultaneously.

Step 5: Check for a stable phase lock. If the vectors of Channel B are not stable, the color genlocking circuitry is not functional and the board should be repaired. Refer to Paragraph 4.9.

4.8.5 Verification of Outputs to Main Logic Board

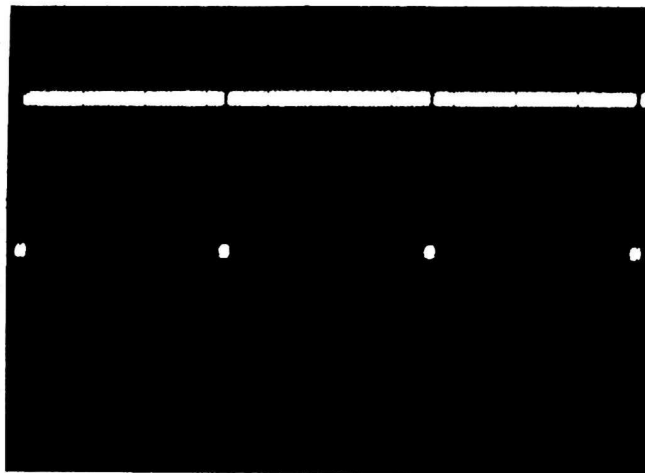
Follow this procedure if there is any question about the Sync Gen/Encoder board's outputs to the Main Logic board.

Step 1: (a) Using the oscilloscope, check J1 pin 3 for the 28 MHz bit clock signal. If the 28 MHz bit clock signal is present, inspect the 34-wire ribbon cable and its connectors. If necessary, replace the cable.

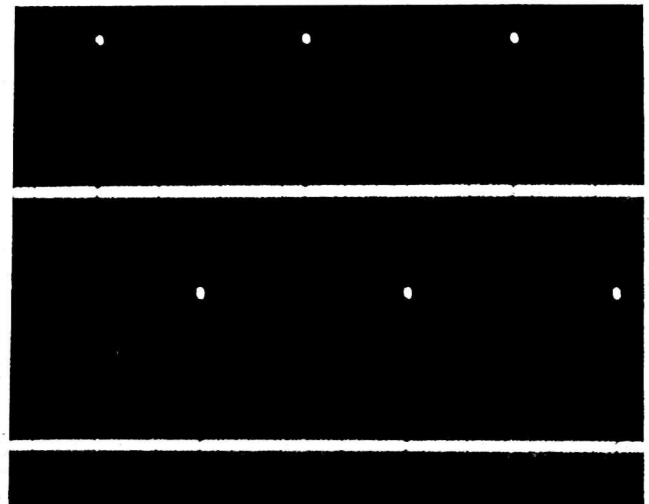
(b) Check U4 pin 4 on the Dual Oscillator board for the 28 MHz clock signal. If this signal is present, inspect the Dual Oscillator P. C. Board. Check the two sets of DIP pins used to connect the board to the Sync Gen/Encoder board. Remove the board, clean the pins with alcohol and a lint-free cloth, and replace the board.

(c) If the bit clock signal is not restored, the Sync Gen/Encoder board is faulty and requires factory repair. Refer to Paragraph 4.9 for board removal instructions.

- Step 2: (a) Place the oscilloscope probe at J1 pin 25. Compare this V-Drive signal with the waveform shown in Figure 4-7, Waveform A. If this signal is present, go on to step 3.
- (b) Inspect U47 for damage or shorts. Trace the signal path on the schematic diagrams (Figure 7-5, 7-6) and look for crossed lines, etc. Check the seating of all socketed chips, especially U44, U52, and U59. If no anomalies are discovered, and the board is not operational, return it to CHYRON® for repair. See Paragraph 4.9.
- Step 3: (a) Using a dual-trace oscilloscope, place one probe on J1 pin 31, and place the other probe on J1 pin 33. Compare these odd- and even-field pulses with the waveform shown in Figure 4-7, Waveform B.
- (b) If these signals are not present, trace the signals on the schematic diagrams and, in turn, on the board. Look for any short circuits or cold solder joints. Check the seating of all socketed chips. If the signals are not restored and the board is not operational, ship the board to CHYRON® for repair. See Paragraph 4.9 for board removal instructions.



Waveform A
V-Drive, @ J1 pin 25
X=0.5us/div Y=0.2v/div



Waveform B
Odd/Even Field Pulses
X=0.5us/div Y=0.2v/div

Figure 4-7. Sync Gen/Encoder Waveforms A, B

4.9 BOARD REMOVAL INSTRUCTIONS

This paragraph describes board removal procedures. All procedures refer to Figure 4-8, VP-2 Physical Exploded View, located at the end of this section.

Several common tools, such as slot head and phillip's head screwdrivers, nut-drivers, and pliers are necessary to complete these procedures.

Several precautions should be taken to avoid the possibility of electrical shock or damage to the VP-2 circuit boards.

- NEVER attempt to work on the VP-2 while the AC power is connected.
- NEVER use force to remove any component of the VP-2.
- BE CAREFUL not to lose small hardware (nuts, bolts, lockwashers) into the VP-2 since these parts could cause short-circuits and damage the unit.
- BE CAREFUL not to damage the corners of the circuit boards while extracting them. Handle all circuit boards with great care.

These procedures list the order in which the VP-2 must be disassembled. The initial disassembly procedure is not necessary when the Sync Gen/Encoder board or the Power Supply are to be removed. Some older units use a bracket-mounted fan that vents through the top of the unit. This fan must be removed before removing the I/O board. The Floppy Disk Drive must be removed before removing the Dual Processor Board or the Main Logic Board. Follow the disassembly order carefully, or else damage to the unit may result.

4.9.1 Initial Disassembly

- Step 1: Remove the four machine screws located on the sides of the unit. (On some older units, the mounting screws are located along the top edges of the cover.) Lift the unit's cover straight up and off.
- Step 2: On some older units, the cooling fan is located on a bracket on the left side of the unit (see Figure 4-8). Remove the two screws that secure the fan/bracket assembly, and lift the assembly out of the unit.

- Step 3: Remove the three machine screws that secure the disk drive unit to the VP-2 chassis. Two of these screws are located on the bottom of the VP-2 chassis, and the third is located on the right side of the chassis. Disconnect the ribbon-cable connector and power connector from the back of the disk drive. Lift the disk drive out of the unit.
- Step 4: If the disk drive itself is to be shipped, remove the three threaded bushings from the disk-drive chassis. Two of the bushings are located on the bottom of the disk drive chassis, and the third is located on the side of the disk drive chassis.

4.9.2 Dual Processor Board Removal

- Step 1: Loosen and remove the two screws that fasten both ends of the hold-down bar to the chassis.
- Step 2: Disconnect the 60-line ribbon cable connector from P1.
- Step 3: Disconnect the power connector from the lower left corner of the board.
- Step 4: Remove the six screw/bushing fasteners that hold down the board. Note the positions of washers and bushings, and be careful not to lose parts.
- Step 5: Grasp the board from the left and right edges. Gently lift the board straight up, and do not rock the board from side to side to work it loose. **DO NOT USE FORCE!** The pins on the underside of the board are fragile.

CAUTION!!!

When handling the board, protect the connector pins located on the solder side. Do not place the board on a flat surface solder-side down without ensuring the safety of the pins. A small chunk of styrofoam, if available, gives the pins excellent protection if placed over the pins.

To re-install the board, reverse the removal procedure. **BE SURE THE CONNECTOR PINS ARE PROPERLY ALIGNED!**

4.9.3 Font Memory Board Removal

- Step 1: Release all font chips from their sockets. Use a flat-blade screwdriver to turn the zero-insertion force socket cams to the "open" position, and remove the font chips. Place the fonts in conductive foam, and store in a static-free place.
- Step 2: Disconnect the 60-line ribbon cable connector from J1.
- Step 3: Remove the +5v power wire from the lug marked "+5".
- Step 4: Remove the 15-line ribbon cable connector from J2.
- Step 5: Remove the six screws that fasten the Font Memory board to the front panel. Note the positions of washers, etc. Remove the board.

To re-install the board, reverse the removal procedure.

4.9.4 I/O Board Removal

- Step 1: Remove the two bolts that fasten the hold-down bar to the VP-2 chassis.
- Step 2: Remove the 34-pin ribbon cable connector from J2 on the right side of the board.
- Step 3: Label and remove the three cable connectors from J4. Be sure to label each wire's destination.
- Step 4: Locate the power cable near the back left side of the board. The power cable is a black-and-red twisted wire pair. Follow the twisted pair and locate a 2-pin inline power connector. Disconnect this power connector.
- Step 5: Remove the five screws that fasten the I/O board to the chassis. Note the placement of the washers, and be careful not to lose parts.
- Step 6: Grasp the board at the left and right edges. Gently lift the board straight up. Rock the board from left to right to free the connector on the underside of the board.

To re-install the board, reverse the removal procedures. Be sure that the connector is properly seated in its socket on the Main Logic P. C. Board.

4.9.5 Main Logic Board Removal

- Step 1: Follow (B) and (D) above to remove both the Dual Processor Board and the I/O Board.
- Step 2: Disconnect the 34-wire ribbon cable connector from J4, near the back right corner of the board.
- Step 3: Disconnect the 4-wire power supply connector from C1 near the back left corner of the board.
- Step 4: Disconnect the 2-wire connector from J6, near the middle of the rear edge of the board.
- Step 5: Using either fingertips or small pliers, squeeze the five nylon stand-off fasteners one at a time, while gently lifting the board. (Some VP-2 units do not use nylon standoff fasteners, but use threaded hardware instead.)

To re-install the board, reverse the removal procedure. When the board has been fastened, check the seating of all socketed chips.

4.9.6 Sync Gen/Encoder Board Removal

- Step 1: Remove the 34-wire ribbon cable connector from J1, near the front right corner of the board.
- Step 2: Remove the 4-wire power connector from J2, at the left edge of the board.
- Step 3: Remove the 16-wire ribbon cable connector from J3, at the left edge of the board.
- Step 4: Remove the 2-wire connector from J8, near the left edge of the board.
- Step 5: Label and remove the cable between J9 and the Program "B" Out connector.
- Step 6: Label and remove the cable between J4 and the Video In connector.
- Step 7: Label and remove the cable between J5 and the Program 'A' Out connector.

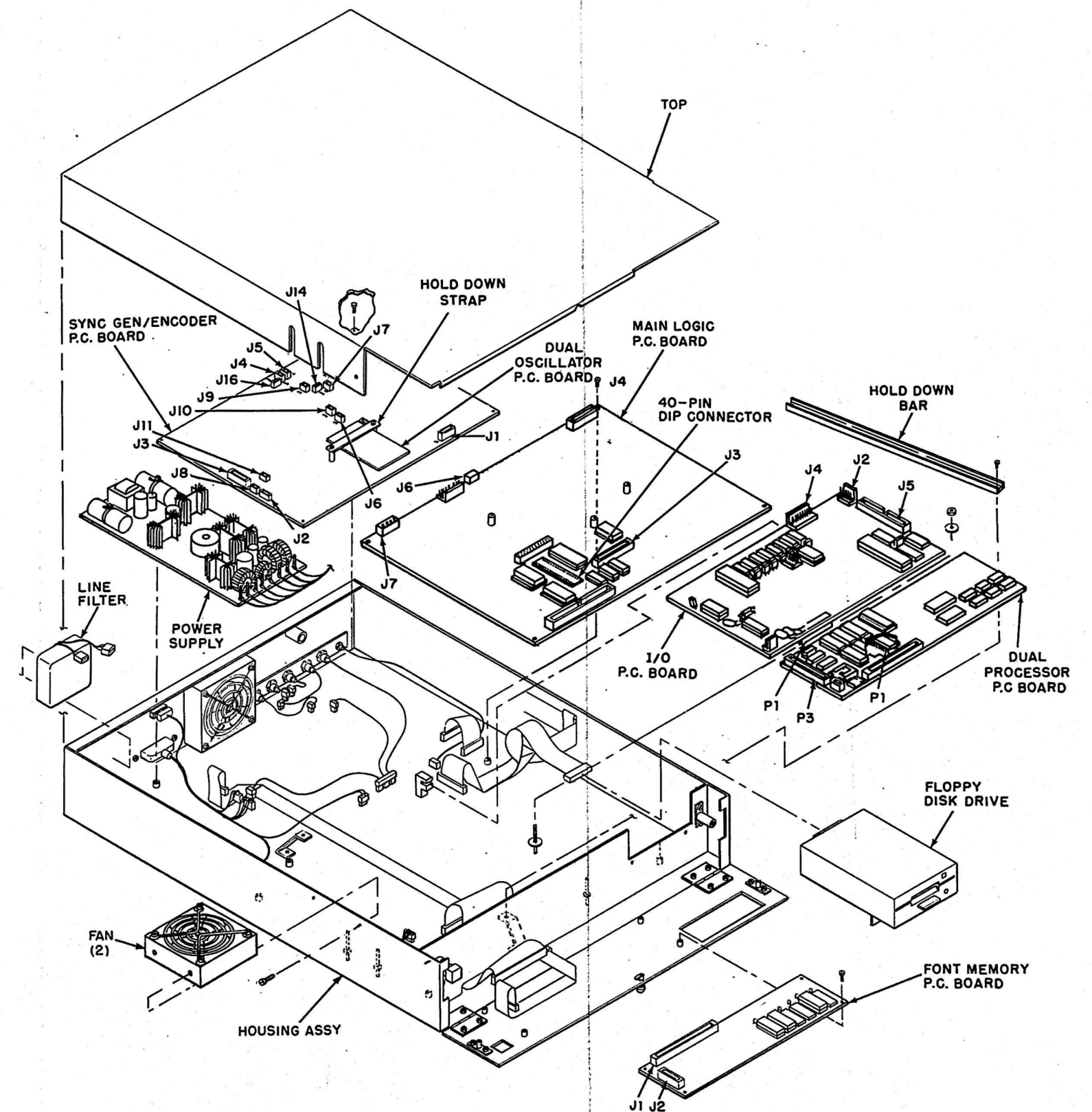
- Step 8: Label and remove the cable between J16 and the Key Out connector.
- Step 9: Remove the Dual Oscillator Board hold-down strap by squeezing the nylon standoff fasteners one at a time and lifting.
- Step 10: Remove the Dual Oscillator Board by grasping the left and right sides and lifting straight up. Be careful not to damage the connecting pins.
- Step 11: Remove the Sync Gen/Encoder Board by squeezing each of the six nylon standoff fasteners and lifting. (Some units use threaded hardware and nylon standoffs, while others use only threaded hardware.)

To re-install the board, reverse the removal procedure. Take care not to damage the pins on the Dual Oscillator board, and to connect all video cables to their proper sources.

4.9.7 Power Supply Removal

- Step 1: Look closely at how the power supply harness is run through the unit. Label each cable with its destination. Some units have the harness connectors labeled in indelible ink. These labels are: P2, to the Sync Gen/Encoder Board; P3, to the I/O Board; P7, to the Main Logic Board; P9, to the AC power filter; and P12, to the Dual Processor Board. One other harness destination is the disk drive, which is not labeled.
- Step 2: Label and remove each of the above harness connectors. Be sure each cable is marked to facilitate re-installation.
- Step 3: Remove the four pan-head screws from the corners of the power supply.
- Step 4: GENTLY lift the power supply, and remove the power-supply harness from the unit.

To re-install, reverse the previous steps.



VP-2 Assembly
Exploded View
Figure 4-8

4.10 SHIPPING INSTRUCTIONS

NOTE

Please contact your dealer or the CHYRON Customer Service department for specific instructions on how to arrange for board shipment/return. Please do not return any material without a Material Return Authorization (MRA).

4.10.1 General Packing Guidelines

Boards must be securely packed before shipment. **REMEMBER!!! IT IS BETTER TO USE A BOX THAT'S A LITTLE BIG THAN TO USE A BOX THAT'S A LITTLE SMALL!!!**

Use a lot of shock-absorbing packing material, such as styrofoam peanuts or foam-rubber blocks. Protect the edges of all boards, and, in the case of the Dual Processor Board and the Dual Oscillator Board, use styrofoam blocks to protect the pins on the bottom of the boards.

Seal each box with sturdy filament packing tape. (It's better to use too much than too little...) Seal the box well enough to withstand rough handling. Mark each box "ELECTRONIC EQUIPMENT--- FRAGILE!"

4.10.2 General Shipping Instructions

Contact the CHYRON customer service department for a MRA, and for any other shipping information. The address is CHYRON CORPORATION, Customer Service Department, 5 Hub Drive, Melville, NY 11747. The telephone number is (516) 249-3018.

Send boards by registered/insured mail.

Feel free to contact the CHYRON Customer Service Department with any questions, or for any additional information.

SECTION 5

Video Alignment Procedure

5.1 INTRODUCTION

The Sync Gen/Encoder section of the VP-2 is fully aligned at the CHYRON® factory before each unit is shipped. However, the VP-2 may occasionally require minor internal adjustments in order to ensure proper video operation.

The following test equipment is required in order to properly complete this video alignment procedure:

Test Generator (RS-170 Broadcast Standard)
Dual Trace Oscilloscope w/ probes
Digital Voltmeter
Waveform Monitor
Vectorscope
Non-metallic Adjustment Tool for Capacitors

The following table lists all of the factory adjustments on the Sync Gen/Encoder/P. C. Board.

Table 5-1. Factory Preset Adjustments

<u>Adjustment Function</u>	<u>PC Board Screening</u>	<u>Component Number</u>
Vertical Phase	VERT PHASE	R236
Center Frequency	CENTER FREQ	C96
Subcarrier Frequency	SUBC FREQ	R219
Encoder Gain	ENCODER GAIN	R48
V Axis Gain	V AXIS GAIN	R14
U Axis Gain	U GAIN (see text)	R226 (R4)
Program Gain	PROGRAM GAIN	R49
Program D. C.	PROGRAM DC	R50
Program HF	PROGRAM HF	C28
Insert Gain	INSERT GAIN	R52
Insert D. C.	INSERT DC	R53
Insert HF	INSERT HF	C32
Chroma Gain	-----	C15

5.2 ADJUSTMENT PROCEDURE

This procedure should be followed using the sequence below, or improper alignment may result. Location numbers in parentheses indicate the board location for each adjustment as shown in Figure 5-1 at the end of this section.

NOTE: If the Video Encoder Board is equipped with C25 as a variable capacitor, this must be adjusted first. Connect a vectorscope to the VP-2 during the power-up diagnostic display. Adjust C25 (Location 1) using a non-metallic tool for maximum amplitude of the Chroma signal without white or black level distortion.

5.2.1 Vertical Phase

1. Connect a test generator (RS-170A standard) composite video signal (i.e., Black Burst) to the VP-2 Video In connector.
2. Externally trigger a dual trace oscilloscope to vertical drive from the test generator.
3. Connect a x10 probe from one channel of the oscilloscope to TP6 REF CSP (Location 2) and connect a x10 probe from the other channel to J11 pin 2 (Location 3).
4. Adjust the oscilloscope so as to view both channels for about 15 lines of the vertical interval (preferably in the "chopped" mode).
5. Adjust vertical phase R236 (Location 4) and observe on the oscilloscope that the sync on J11 pin 2 moves in steps of 1/2 line with respect to the sync on TP6.
6. Adjust R236 so that the sync is 1/2 line early; note the potentiometer setting and then re-adjust R236 so that the sync is 1/2 line late. The final setting for R236 is midway between these two settings.

5.2.2 Center Frequency

1. With the VP-2 genlocked to an RS-170A video source, monitor U38 pin 6 (Location 5) with either an oscilloscope or a digital voltmeter.
2. Set the oscilloscope vertical deflection to 2 volts/division and the horizontal deflection to 20 microseconds/division, externally triggered to the test generator sync.
3. Adjust C96 (Location 6) for approximately 6 volts at U38 pin 6.

5.2.3 Subcarrier Frequency

1. Set the oscilloscope vertical deflection to 2 volts/division and the horizontal deflection to 20 microseconds/division, externally triggered to the test generator sync.
2. Remove the RS170A video source from the VP-2 Video In channel.
3. Adjust R219 (Location 7) until the voltage at U38 pin 6 is the same voltage as in Step B-3 above.

5.2.4 Encoder Gain

1. Using a digital voltmeter, monitor U16 pin 3 (Location 8) and adjust DAC reference R48 (Location 8) for 2.80 VDC.
2. Create a color-bar display on the VP-2 by calling up the palette menu, or by composing any display that uses all eight of the on-screen colors. (Any display that contains all eight default colors (Black, Blue, Green, Cyan, Red, Magenta, Yellow, and White) will suffice as a test display for this alignment step.)
3. Monitor the Preview Out/Edit Out channel with a properly calibrated waveform monitor and verify that the luminance is within 2% of nominal levels. Slight re-adjustment of R48 is permissible in order to achieve this condition.
4. Monitor the Program Out B channel with a vectorscope. Set R226 (Location 9) and R14 (Location 10) to approximately center range. Adjust C15 (Location 11) using a non-metallic tool for correct amplitude indicated by the 5-degree alignment boxes on the vectorscope.

5.2.5 V Axis Gain (Chroma Gain)

1. Monitor the Program Out B channel with the vectorscope and adjust the V Axis Gain potentiometer R14 (Location 10) so that vectors lying close to the V axis are located within the 5-degree boxes on the vectorscope.

5.2.6 U Axis Gain

NOTE: On some earlier versions of the Sync Gen/Encoder board, the U Axis Gain potentiometer has the designation R4, without the "U GAIN" screening. The adjustment is at the same location on all editions of the board.

1. Monitor the Program Out B channel with the vectorscope and adjust the U Axis Gain potentiometer R226 (Location 9) so that vectors lying close to the U axis are located within the 5-degree boxes on the vectorscope.

NOTE: Slight re-adjustment of V Axis Gain (5.2.5) may be necessary to achieve correct phase and amplitude.

5.2.7 Program Gain

1. Connect a calibrated 10 MHz sweep video signal to the Video In channel and monitor the Program Out A channel with a vectorscope and a waveform monitor.
2. Monitor Program Out test point TP3 (Location 12) with one channel of the oscilloscope. Set the oscilloscope vertical deflection to 0.5 volt/division and horizontal deflection to 20 microseconds/division. Trigger the oscilloscope externally to test point TP6 (REF CSP, Location 2).
3. While monitoring Program Out A with the waveform output, adjust PGM Gain potentiometer R49 (Location 13) for correct output signal level (1.0 volt p-p).

5.2.8 Program DC

1. While monitoring PGM Out TP3 with the oscilloscope as in the previous step, adjust PGM DC R50 (Location 14) so that video blanking level is at 0 volt.

5.2.9 Program HF

1. While monitoring Program Out A with the waveform monitor, adjust PGM HF C28 (Location 15) for flat response (minimum null point).

5.2.10 Insert Gain

1. Set up the VP-2 to produce the Color Bar test pattern described previously. Fully key in the insert video.
2. Monitor the Program Out A channel and test point TP3 as in (5.2.7) above. Adjust the Insert Gain potentiometer R52 (Location 16) for correct video amplitude on the waveform monitor (1.0 volt P-P; 140 IRE).

5.2.11 Insert DC

1. Monitor PGM OUT test point TP3 with the oscilloscope as in (5.2.8), and adjust Insert DC potentiometer R53 (Location 17) so that the Black Bar is set to 7.5 IRE.
2. Re-check step 5.2.10 and re-adjust as necessary. Then re-check step 5.2.11.

5.2.12 Insert HF

1. Monitor the Video Out A channel with the vectorscope and adjust the Insert HF C32 (Location 18) so that the BAR vectors are the correct amplitude.

5.3 USER ADJUSTMENTS CHECK

Four adjustments are provided to allow for timing the VP-2 into a system containing other video signals. These adjustments are only active during Genlock operation. All user adjustments are located on the left side of the Font P. C. Board behind the VP-2 front panel.

5.3.1 Horizontal Phase

This adjustment allows the user to horizontally time the unit with reference to the external video present on the Video In channel. There are approximately ± 1.5 microseconds of adjustment available.

5.3.2 Coarse Subcarrier Phase

The Subcarrier Phase of the insert video may be adjusted in steps of 90° with respect to the external video present on the Video In channel by means of a four-position jumper clip.

5.3.3 Fine Subcarrier Phase

A continuous adjustment of subcarrier phase is available to provide a fine range of subcarrier phase adjustment. There are approximately 110° of adjustment across each quadrant.

5.3.4 Key Mix Rate

The user may adjust the rate at which a key is mixed over a background video signal. The approximate transition duration is adjustable from 0 to 3 seconds.

5.3.5 Key Timing Adjust

The user may adjust the timing of the VP-2 key output in relation to Program 'B' Out when using the unit in conjunction with an external keyer. The unit is shipped with this adjustment set at the "test" position, in order to produce coincident signal outputs from the Program "B" Out channel and the Key Out channel.

Routing these signals into a switcher matrix introduces a delay. This delay may be compensated for by moving the jumper wire connecting U7 pin 1 on the Sync Gen/Encoder P.C. Board to any of the following pins on U4:

- TO ADVANCE TIMING (in 35 ns steps): 6,5,4,3
- TO RETARD TIMING (in 35 ns steps) : 10,11,12,13

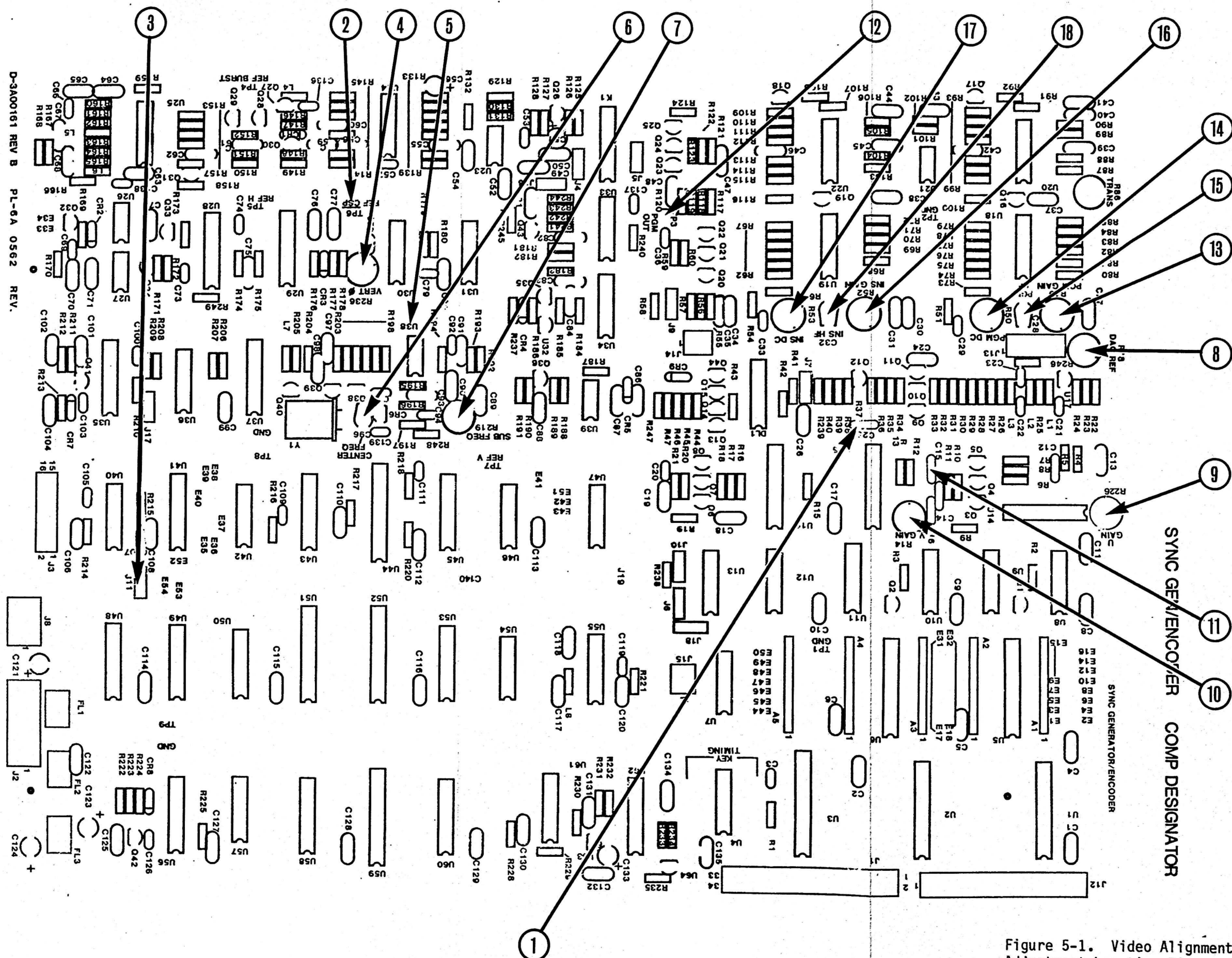


Figure 5-1. Video Alignment Adjustment Location Diagram 5-7/5-8

SECTION 6

Parts Lists

6.1 INTRODUCTION

This section contains parts lists for each P. C. board in the VP-2 unit. These Lists are, however, limited to listings of the integrated circuits within the unit and other parts that require exact replacements. CHYRON® assumes that any other parts (including resistors and capacitors) are readily available to the technician. Therefore for brevity's sake, common parts are not included in these lists.

6.2 COMPLETE ASSEMBLIES

<u>DESCRIPTION</u>	<u>CHYRON® PART NUMBER</u>
Dual Processor P. C. Board Ass'y	6A00559
Font Memory P. C. Board Ass'y	6A10507
Main Logic P. C. Board Ass'y	6A10509
I/O P. C. Board Ass'y	6A00567
Sync Gen/Encoder P. C. Board Ass'y	6A00562
Dual Oscillator P. C. Board Ass'y	6A00585
Micro Floppy Disk Drive Ass'y	15A0009
Power Supply Ass'y	2C00897

6.3 DUAL PROCESSOR P. C. BOARD

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U1	1-of-4 Decoder/Demultiplexer	74LS155	06F0028
U2	Octal Latch	8282	06J0022
U3	Same as U2		
U4	16-Bit Microprocessor	80186	6A00575
U5	Bipolar Memory	2186A-25	06P0013
U6	Same as U5		
U9	ROM, Programming		3F00435
U10	ROM, Programming		3F00436
U12	Octal Bus Transceiver	74LS245	06F0065
U13	Same as U12		
U14	8-Bit Microprocessor	8088-2	06M0001
U15	Same as U12		
U16	Same as U12		
U17	Quad 2-Input NOR Gate	74F32	06C0114
U18	Bus Controller	8288	06P0014
U19	Same as U2		
U20	Quad 2-Input Multiplexer	74LS257	06F0071
U21	Quad 2-Input NAND Gate	74F00	06C0102
U22	2k-by-8 Static RAM	TC-5565PL-15	06K0025
U23	Same as U22		
U24	Dual D-type Flip-Flop	74LS74 (TI only)	06F0016
U25	Hex Inverter	74F04	06C0104
U26	Quad 2-Input Multiplexer	74F157	06C0065
U27	Same as U26		
U28	Same as U17		
U29	Same as U21		

Dual Processor P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U30	One-Shot	74LS221	06F0054
U31	Same as U26		
U32	Same as U26		
U33	Triple 3-Input NOR Gate	74LS27	06F0009
U34	Same as U21		
U35	Quad 2-Input NOR Gate	74LS32	06F0014
U36	Quad 2-Input NOR Gate	74F02	06C0103
U37	Same as U17		
U38	Dual D-Type Flip-Flop	74F74	06C0106
U39	Quad 2-Input AND Gate	74F08	06C0105

6.4 FONT MEMORY P. C. BOARD

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U1	PROM		3F00412
F1	Font PROM 30-Line Helvetica Bold		3F00320
F2	Font PROM 18-Line Helvetica Medium		3F00319
--	Zero Insertion Force Sockets 228-4845-00-3307		18B0001

6.5 MAIN LOGIC P. C. BOARD

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U1	Bi-Polar Memory	HM 6167 HP-55	06P0012
U2	Same as U1	(or equivalent)	
U3	Same as U1		
U4	Same as U1		
U5	Same as U1		
U6	Same as U1		
U7	Same as U1		
U8	Same as U1		
U9	RS232 Receiver	AM1488	06N0001
U10	Same as U1		
U11	Same as U1		
U12	Same as U1		
U13	Same as U1		
U14	Same as U1		
U15	Same as U1		
U16	Same as U1		
U17	Same as U1		
U18	Quad 2-Input Multiplexer	74F157	06C0109
U19	Quad D-type Flip-Flop	74F175	06C0110
U20	Same as U1		
U21	Same as U1		
U22	Same as U1		
U23	Same as U1		
U24	Same as U1		
U25	Same as U1		
U26	Same as U1		
U27	Same as U1		
U28	RS232 Driver	AM1489	06N0002
U29	Same as U1		
U30	Same as U1		
U31	Same as U1		
U31	Same as U1		
U32	Same as U1		
U33	Same as U1		
U34	Same as U1		
U35	Same as U1		
U36	Same as U1		

Main Logic P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U37	Same as U18		
U38	Dual J-K Flip-Flop	74F109	06C0107
U39	Octal D-Flip-Flop	74LS374	06F0064
U40	Same as U39		
U41	Presettable Binary Counter	74F163	06C0113
U42	Same as U41		
U43	Same as U18		
U44	Same as U18		
U45	Same as U18		
U46	Same as U18		
U47	Same as U18		
U48	Quad 2-Input NAND Gate	74F00	06C0102
U49	Hex Inverter	74F04	06C0104
U50	Same as U39		
U51	Same as U39		
U52	Same as U41		
U53	Same as U41		
U54	Same as U18		
U55	Same as U18		
U56	Same as U18		
U57	Same as U18		
U58	Quad 2-Input Multiplexer	74LS257	06F0071
U59	Same as U58		
U60	Dual D-Type Flip-Flop	74F74	06C0106
U61	Bi-Polar Memory	2186A-25	06P0013
U62	Same as U61		
U64	1-of-8 Decoder/Demultiplexer	74F138	06C0108

Main Logic P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U67	Same as U64		
U68	Interrupt Controller	8259A	06J0021
U69	Quad 2-Input AND Gate	74LS08 (TI only)	06F0004
U70	4-Bit Latch	74LS375 (TI only)	06F0061
U71	Quad 2-Input AND gate	74F08	06C0105
U74	Bi-Directional Counter	74LS169 (TI only)	06D0018
U75	Same as U74		
U76	Static RAM	74S189	06D0050
U77	Same as U76		
U78	Same as U64		
U79	Clock Generator	8284A(Intel only)	06J0023
U80	Quad 2-Input NAND Gate	74LS00	06F0001
U81	4-Bit Comparator	74LS85	06F0026
U82	Quad 2-Input OR Gate	74LS32	06F0014
U83	Triple 3-Input NOR Gate	74LS27	06F0009
U84	Quad Bus Buffer Gate	74LS125	06F0021
U85	Same as U18		
U86	Same as U74		
U88	Same as U76		
U89	Same as U61		
U90	ROM Programming		3F00923

Main Logic P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U91	ROM Programming		NTSC: 3F00924 PAL: 3F00925
U92	Octal Latch	8282	06J0022
U93	Same as U70		
U94	Same as U69		
U95	Hex Inverter	74LS04	06F0003
U96	US/ART	8251A	06J0020
U97	Dual Decade Counter	74LS390	06C0112
U98	Dual Modulo-16 Counter	74LS393	06F0049
U99 U100	Quad 2-Input NOR Gate Same as U99	74F02	06C0103
U101	Same as U48		
U102	Same as U49		
U103	Same as U48		
U104	4-Bit Shift Register	74F194	06C0111
U105 U106 U107	Same as U48 Same as U48 Same as U48		
U108	Quad 2-Input NAND Gate	74LS132	06F0053
U109	Dual 1-of-4 Decoder	74LS139	06F0023
U110	Same as U49		
U111	Same as U64		
U112	Same as U109		
U113	Same as U92		
U114	Same as U60		

6.6 I/O P. C. BOARD

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U1*	P.C. mounted beeper	KMB-06	26C09002
U2*	8K x 8 Dynamic RAM	TMS4416	-----
U3*	Same as U2		
U4	Video Display Processor	TMS9918A	06S0011
U4*		TMS9928	
U4†		TMS9929	
U5	16K x 1 Dynamic RAM	8118-12	06K0023
U6	Same as U5		
U7	Same as U5		
U8	Same as U5		
U9	Same as U5		
U10	Same as U5		
U11	Same as U5		
U12	Same as U5		
U13	RS422 Line Receiver Modified w/ 470pf Capacitor	3486	5A00470
U14	Bi-Directional Counter	74S169	06D0018
U15	Hex Inverter	74F04	06C0104
U16	Hex Inverter	74LS04	06F0003
U17	Quad 2-Input NOR Gate	74LS02	06F0002
U18	Quad 2-Input Multiplexer	74157	06C0125
U19	Dual Modulo-16 Counter	74LS393	06F0049

* Parts are only on boards revision 3A0xxx and above.

† Parts are only used in PAL units.

I/O P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U20	Quad 2-Input Schmitt Trigger NAND Gate	74132	06C0086
U21	Dual J-K Negative-Edge Triggered Flip-Flop.	74S112	06D0014
U22	Data Separator	FDC9216B	06S0010
U23	8-MHz Crystal Oscillator	K1115AM	12B0011
U24	Quad D-Type Flip-Flop	74LS175	06F0031
U25	Dual 4-Input Multiplexer	74153	06C0060
U26	Hex Inverter Buffer/Driver	7406	06C0004
U27	Hex Schmitt-Trigger Inverter	74LS14	06F0027
U28	Floppy Disk Controller	8272A	06S0013
U29	Hex 3-State Inverter/Buffer	74LS368	06F0051
U30	One Shot	74LS221	06F0054
U31	Quad 2-Input OR Gate	74LS32	06F0014
U32	8-Input Universal Shift/Storage Register	74S299	06D0034
U33	Dual D-Type Flip-Flop	74LS74	06F0016
U34	Triple 3-Input NOR Gate	74LS27	06F0009
U35	Same as U34		
U36	Dual D-Type Flip Flop	74S74	06D0009

* Parts are only on board revisions D3A00186 and above.

† Parts are only used in PAL units.

I/O P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U39*†	Op-Amp	LM318N	
U40*†	Bilateral Switching Network	4066AE	
U41*†	Op-Amp	LM316N	
U42*†	Same as U41		
Q1	NPN Transistor	2N3904	05T0005
Q2	Same as Q1		
Q3	PNP Transistor	2N3906	05T0006
Q4	Same as Q1		
Q5	Same as Q3		
Q6	Same as Q1		
Q7	Same as Q3		
Q8	Same as Q1		
Q9	Same as Q1		
D1	Diode	1N914	05J0002
D2	Zener Diode	1N5231B	05H0001
D3	Same as D1		
D4	Diode	1N2070	05J0005
D5	Same as D4		
D6*†	Diode	1N914	05J0002

* Parts are only on boards revision D3A00186 and above.

† Parts are only used in PAL units.

6.7 SYNC GENERATOR/ENCODER P. C. BOARD

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U1	Matrix PROM		3F00426
U2	Matrix PROM		3F00427
U3	Matrix PROM		3F00428
U4	Series-to-Parallel Shift Register	74HC164N	06H0027
U5	Octal Buffer	74HC244N	06H0028
U6	Same as U5		
U7	Same as U4		
U8	Quad 2-Input Exclusive OR Gate	74HC86N	06H0021
U9	Same as U8		
U10	Same as U8		
U11	Same as U8		
U12	Quad 2-Input NAND Gate	74HC00N	06H0026
U13	Same as U12		
U14	High-Speed D/A Converter	HI5618B-5	06N0020
U15	Same as U14		
U16	Same as U14		
U17	Shunt Regulator	TL431CLP	06N0021
U18	Dual Op-Amp	CA3054E	06N0022
U19	Same as U18		
U20	NPN Transistor Array	CA3086	06N0017
U21	Linear BiFET Op-Amp	TL081CP	06N0023
U22	Same as U20		
U23	Power Switcher/Amp	CA3094E	
U24	Same as U20		
U25	Comparator	MC1469L	

Sync Generator/Encoder P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U26	Op-Amp (PAL Boards Only)	CA3080E	06N0012
U27	Same as U26		
U28	One-Shot	74LS221	06F0054
U29	Same as U28		
U30	Hex Inverter	74HC04	06H0024
U31	Dual D-type Flip-Flop	74HC74	06H0019
U32	Voltage Regulator	TL068CLP	06N0016
U33	Quad 2-Input Schmitt Trigger NAND Gate	74HC132	
U34	Same as U31		
U35	Same as U28		
U36	Quad Bilateral Switch	CD4066AE	06N0014
U37	Dual J-K Negative Edge Triggered Flip-Flop	74HC112 (TI Only)	06H0021
U38	Quad Op-Amp	CA3140AE	06N0013
U39	Op-Amp	TL082CP	06N0018
U40	Quad 2-Input NOR Gate	74HC02N	06N0030
U41	Same as U37 (PAL Boards Only)		
U42	Same as U37 (PAL Boards Only)		
U43	Up/Down Binary Counter	74HC193N	06H0022
U44		TBP28L22	
U45	Same as U43		
U46	Same as U8		
U47	Same as U40		

Sync Generator/Encoder P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U48	Same as U37		
U49	Same as U37		
U50	Same as U31		
U51	Octal D-Type Flip-Flop	74HC374	06H0022
U52	PAL	10L8	3F00430
U53	Same as U37		
U54	Same as U30		
U56	Same as U28		
U57	Same as U31		
U58	Same as U43		
U59	PROM		3F00431
U60	Same as U93		
U62	Micropower PLL	CD4046AE	06N0015
U63	Same as U32		
U64	Same as U17		
Q1	NPN Transistor	2N5769	05T0036
Q2	Same as Q1		
Q3	PNP Transistor	2N4126	05T0034
Q4	Same as Q3		
Q5	NPN Transistor	2N4124	05T0033
Q6	Same as Q3		
Q7	Same as Q3		
Q8	Same as Q5		
Q11	Same as Q5		
Q12	Same as Q5		

Sync Generator/Encoder P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
Q13	Same as Q3		
Q14	Same as Q3		
Q15	Same as Q5		
Q16	Same as Q5		
Q17	Same as Q5		
Q18	Same as Q5		
Q19	Same as Q5		
Q20	Same as Q3		
Q21	Same as Q3		
Q22	Same as Q5		
Q23	Same as Q5		
Q24	Same as Q3		
Q25	Same as Q5		
Q26	Same as Q5		
Q27	Same as Q5		
Q28	Field Effect Transistor	P1087-18	05T0037
Q29	Same as U28		
Q30	Same as Q5		
Q31	Same as Q5		
Q32	Same as Q5		
Q33	Same as Q3		
Q34	Same as Q3		
Q35	Same as Q5		
Q36	Same as Q28		
Q40	Same as Q1		
Q41	Same as Q3		
Q42	Same as Q3		
Q43	Same as Q5		
DL1	250-ns Delay Line w/ Filter	SP769	26B0006

Sync Generator/Encoder P. C. Board (Cont.)

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
CR1	Diode	1N4148	05J0027
CR2	Same as CR1		
CR3	Same as CR1		
CR4	Same as CR1		
CR5	Zener Diode	1N5234B (Motorola only)	05H0007
CR7	Same as CR1		
CR8	Same as CR1		
A1	SIP Resistor Network, 10Kohm	110A103	01F0032
A2	SIP Resistor Network, 2Kohm	110A202	01F0033
A3	Same as A1		
A4	Same as A2		
A5	Same as A2		
FL1	Power Filter Wide Band Choke	VK200 10/3B	07E0001
FL2	Same as FL1		
FL3	Same as FL1		
L1	Coil, 6.8 Microhenrys		07D0029
L2	Coil, 22 Microhenrys		07D0010
L3	Same as L1		
L5	Same as L2		
L6	Coil, 4.7 Microhenrys		007D0023
L7	Same as L6		
L8	Same as L6		
K1	Subminiature Relay	LM12D00	10A0006

6.8 DUAL OSCILLATOR P. C. BOARD

<u>REFERENCE DESIGNATION</u>	<u>DESCRIPTION</u>	<u>MANUFACTURER'S PART NUMBER</u>	<u>CHYRON® PART NUMBER</u>
U1	Quad Bilateral Switch	CA4066	06M0014
U2	Voltage Controlled Oscillator	74LS624N	06C0116
U3	Quad 2-Input Multiplexer	74F157	06C0109
U4	Hex Inverter	74S04	06D0003
U5	28.6363 MHz Oscillator	K1100A/28.6363	12B0014

SECTION 7

Schematic Diagrams

7.1 INTRODUCTION

This section contains complete schematic diagrams for the VP-2 character generator. Each P.C. board within the unit corresponds to a figure number in this section. For multi-page schematic diagrams, the pages are numbered within the figure.

7.2 CONTENTS

The following schematic diagrams appear in this section:

DUAL PROCESSOR P.C. BOARD SCHEMATICS

Figure 7-1
(sheets 1 - 3)

FONT MEMORY P.C. BOARD SCHEMATICS

Figure 7-2
(one sheet)

MAIN LOGIC P.C. BOARD SCHEMATICS

Figure 7-3
(sheets 1 - 7)

I/O P.C. BOARD SCHEMATICS

Figure 7-4
(sheets 1 - 4)

SYNC GEN/ENCODER P.C. BOARD SCHEMATICS

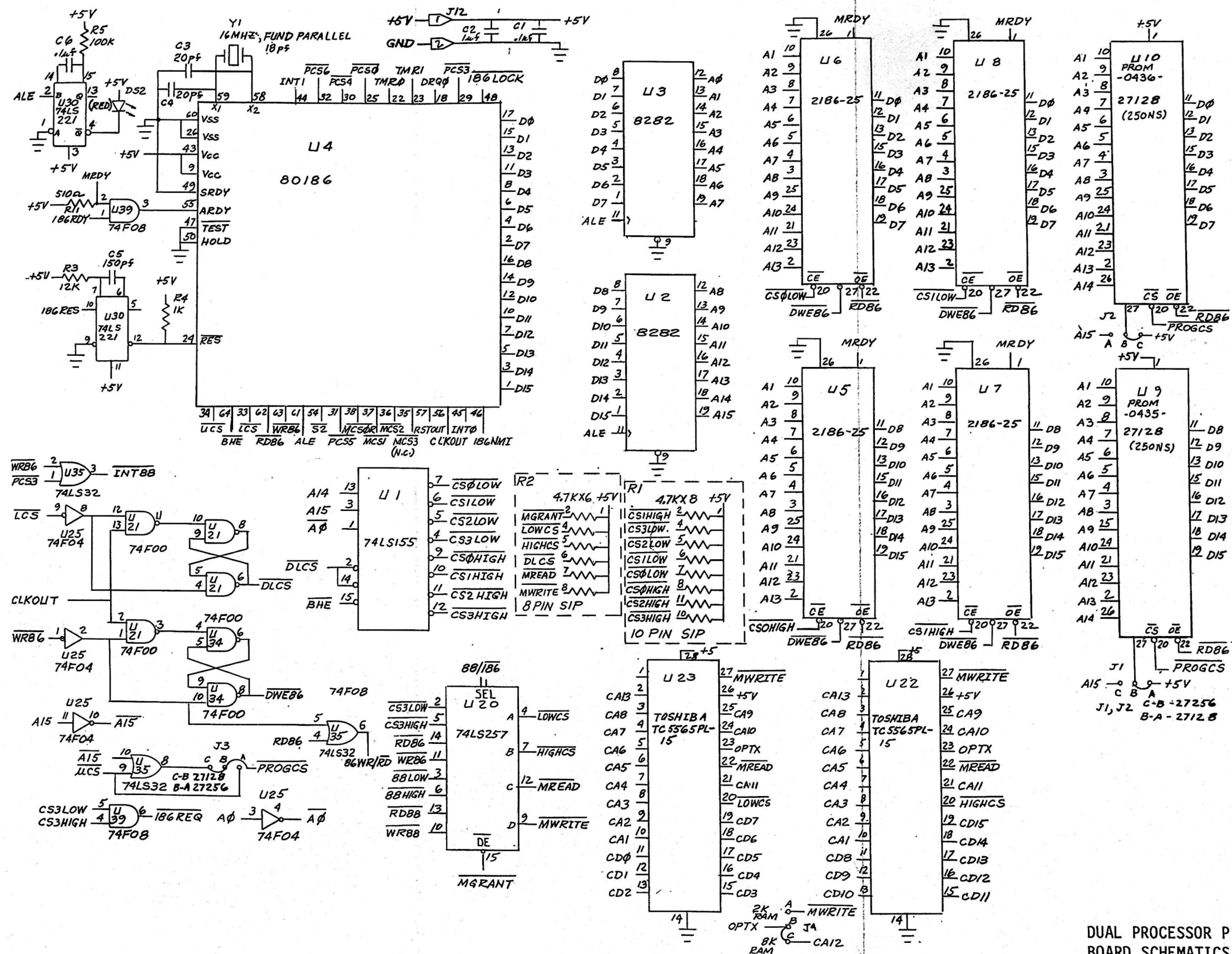
Figure 7-5
(sheets 1 - 7)

DUAL OSCILLATOR P.C. BOARD SCHEMATICS

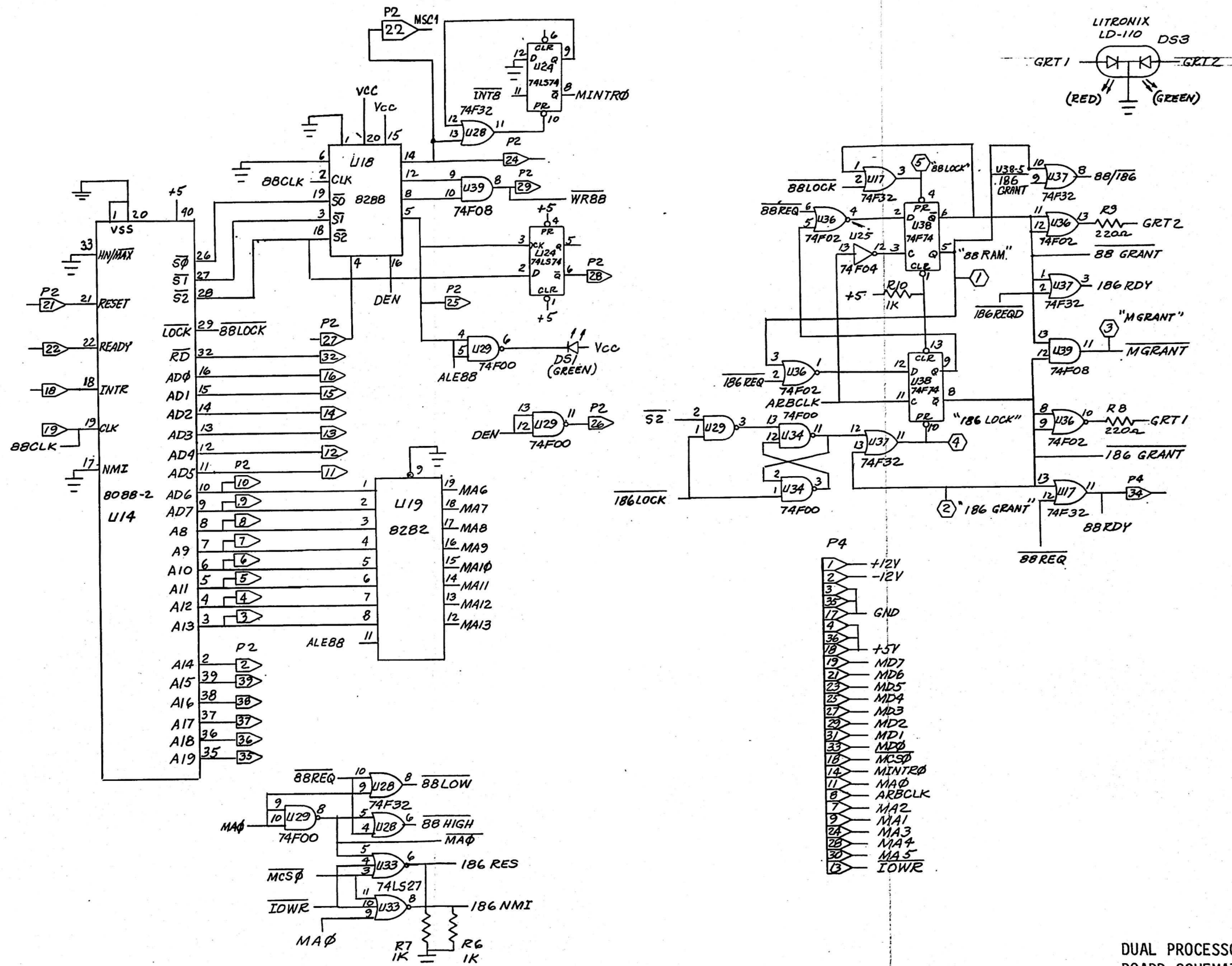
Figure 7-6
(one sheet)

KEYTRONICS KEYBOARD SCHEMATICS

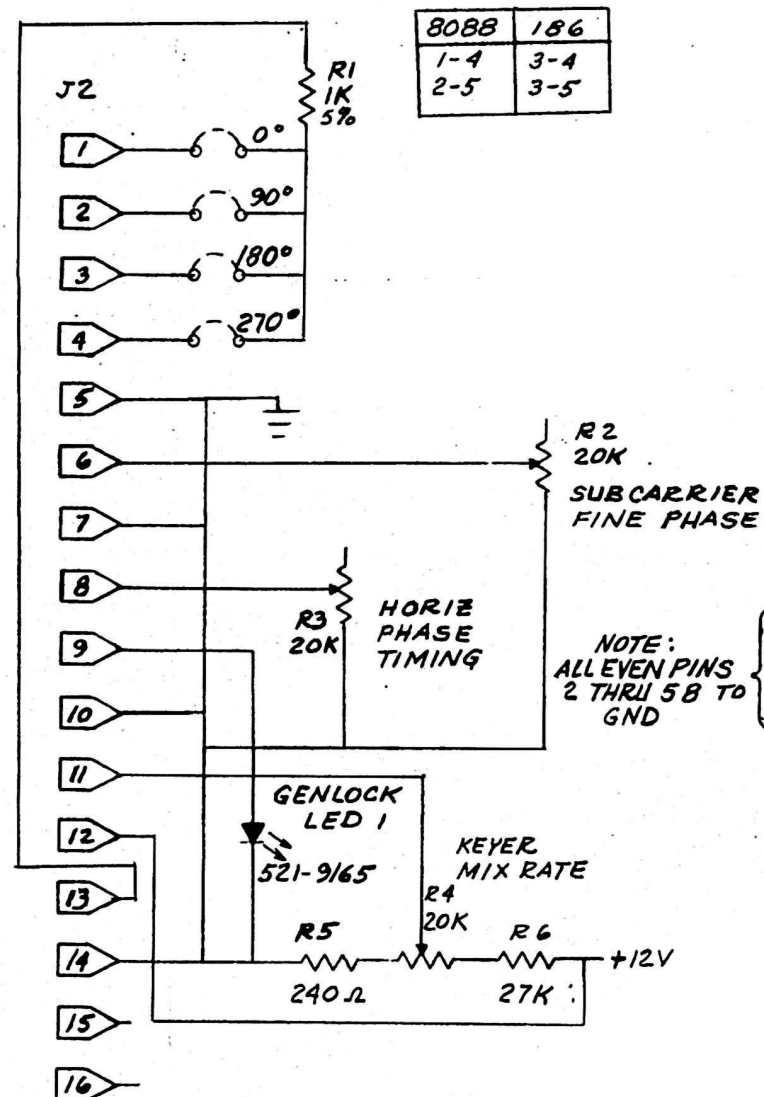
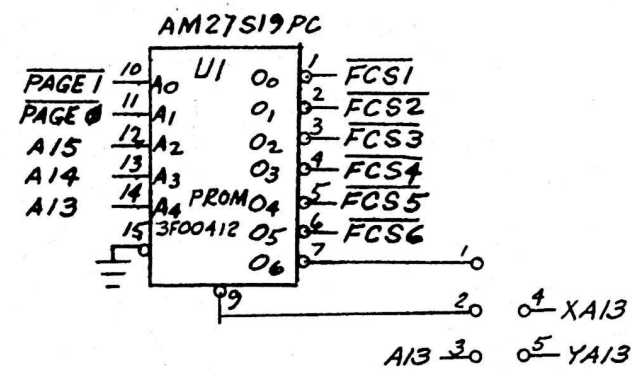
Figure 7-7
(sheets 1 - 2)



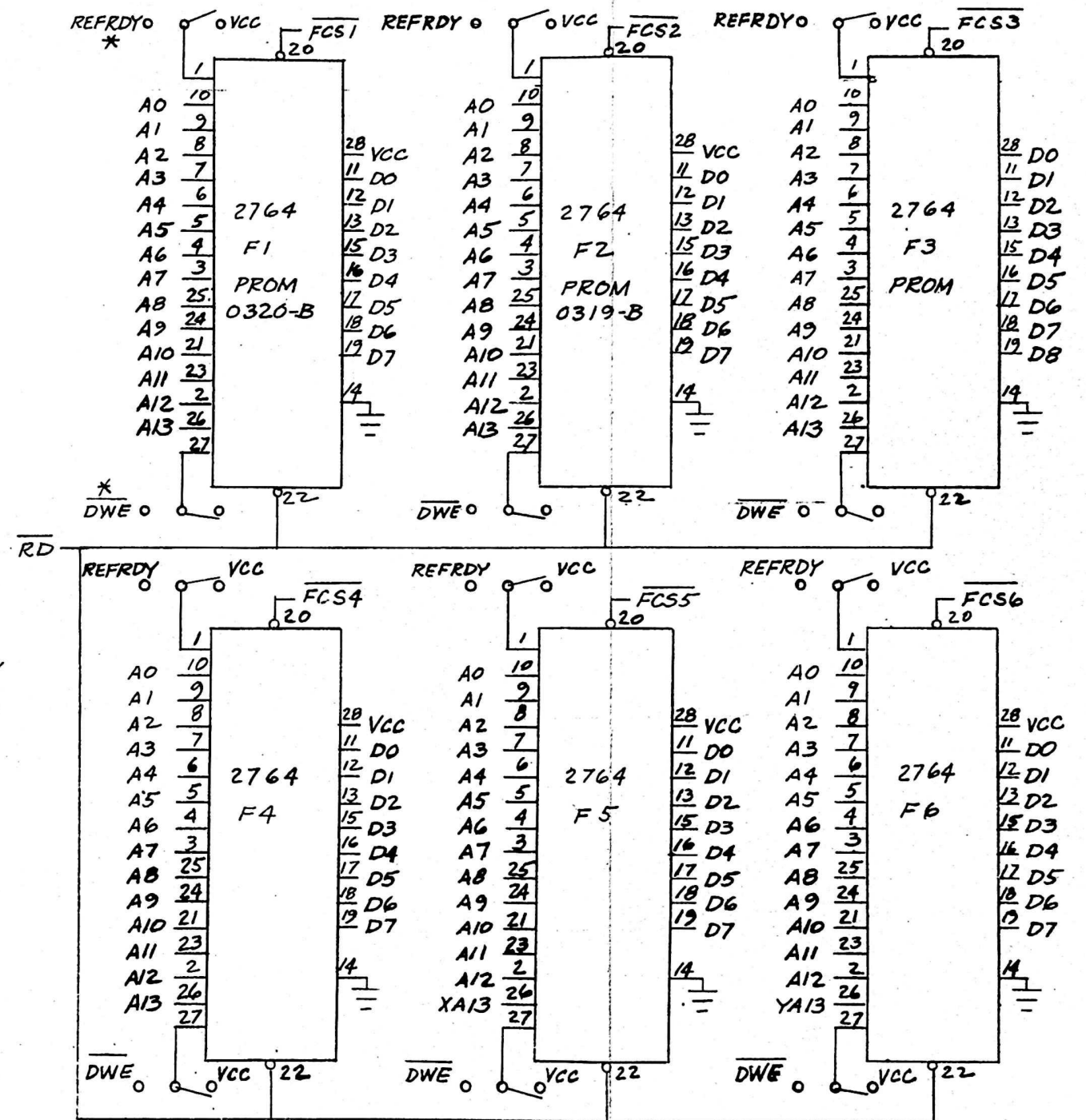
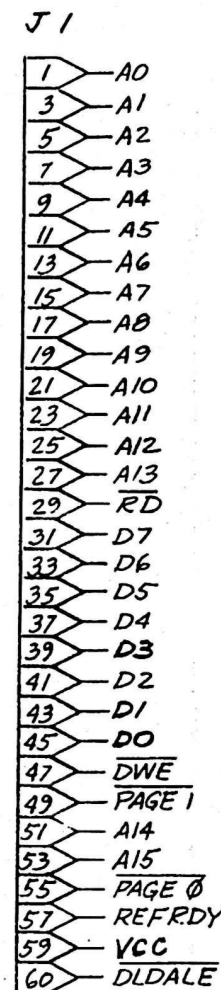
DUAL PROCESSOR P.C.
BOARD SCHEMATICS
Figure 7-1
Sheet 1 of 3



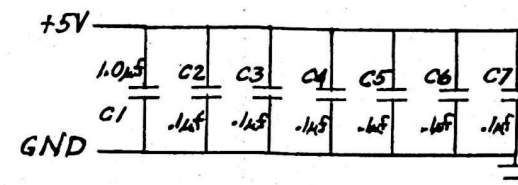
DUAL PROCESSOR P.C.
BOARD SCHEMATICS
Figure 7-1
Sheet 3 of 3

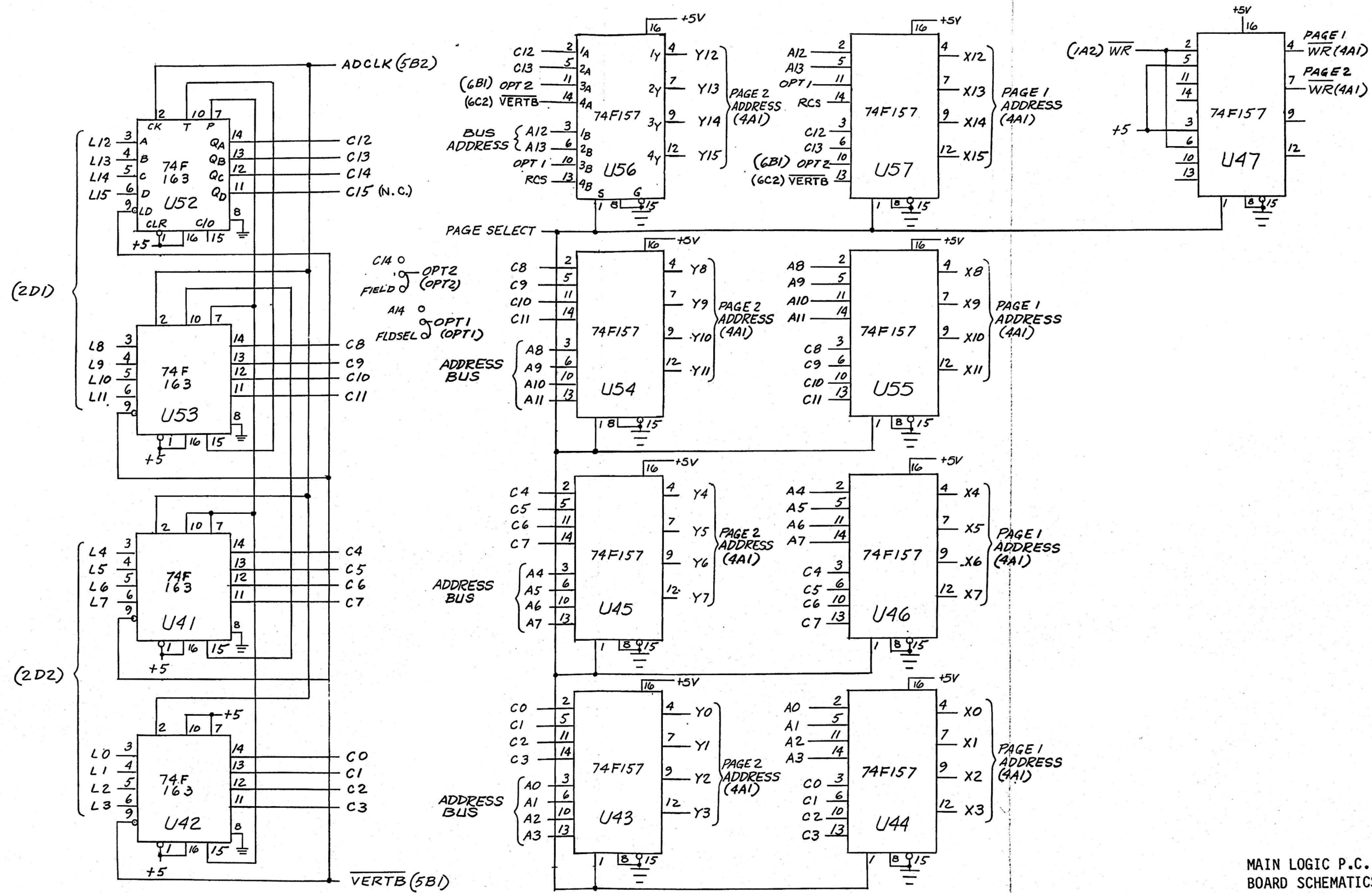


8088	186
1-4	3-4
2-5	3-5



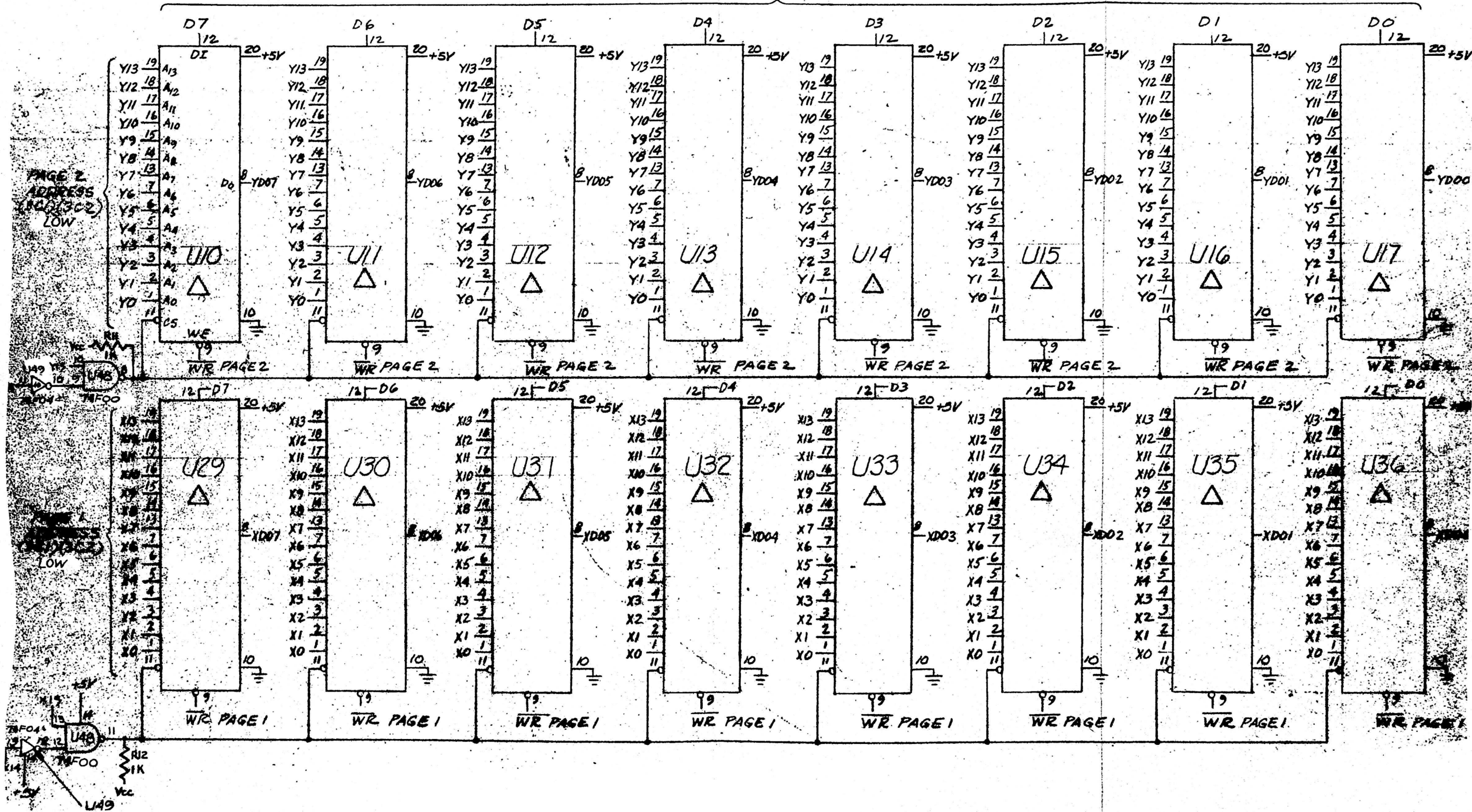
* NOTE:
 SELECT JUMPERS REFRDY AND DWE
 FOR 2186 RAM, ELSE SELECT VCC
 FOR 2764 & 27128 TYPE EPROM



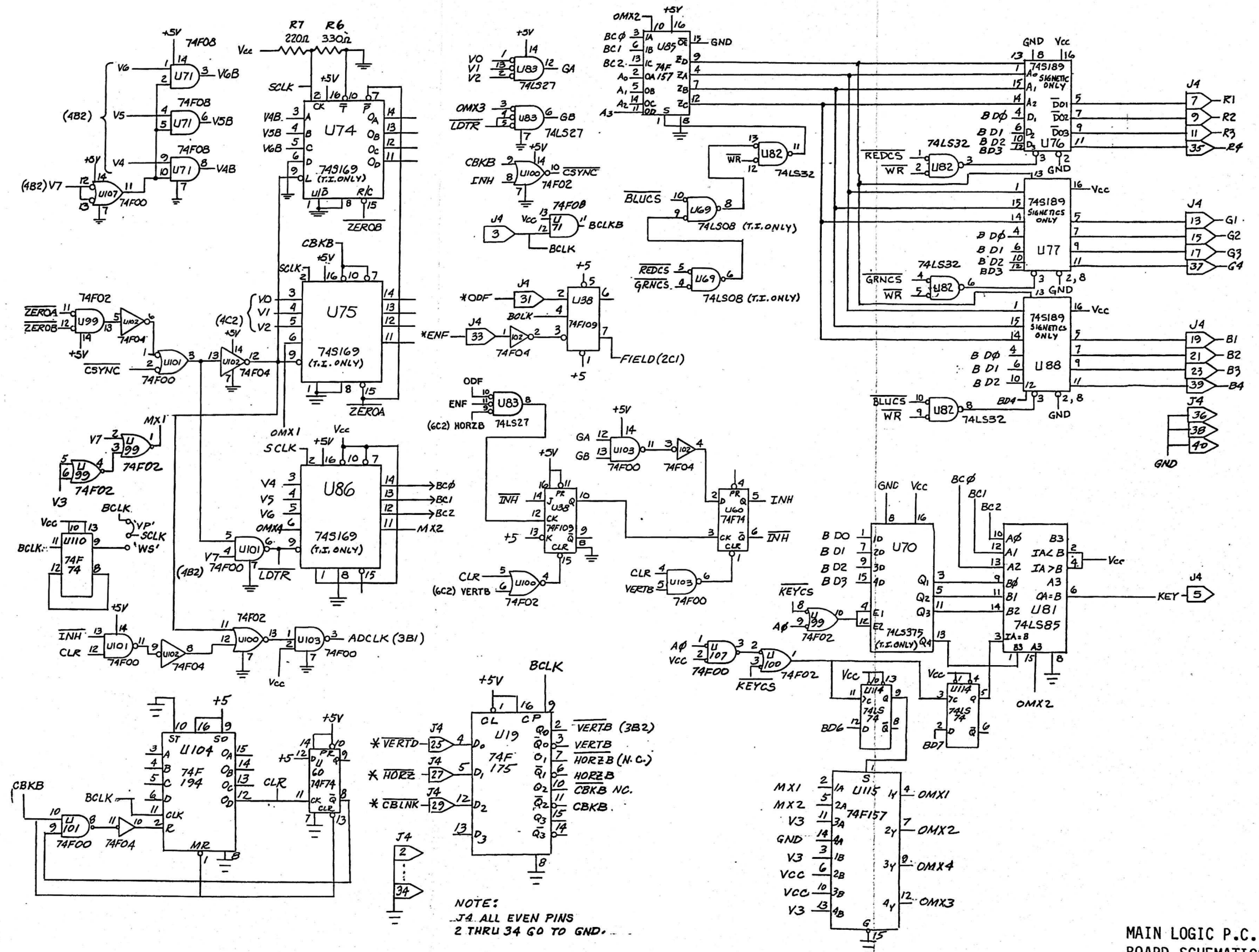


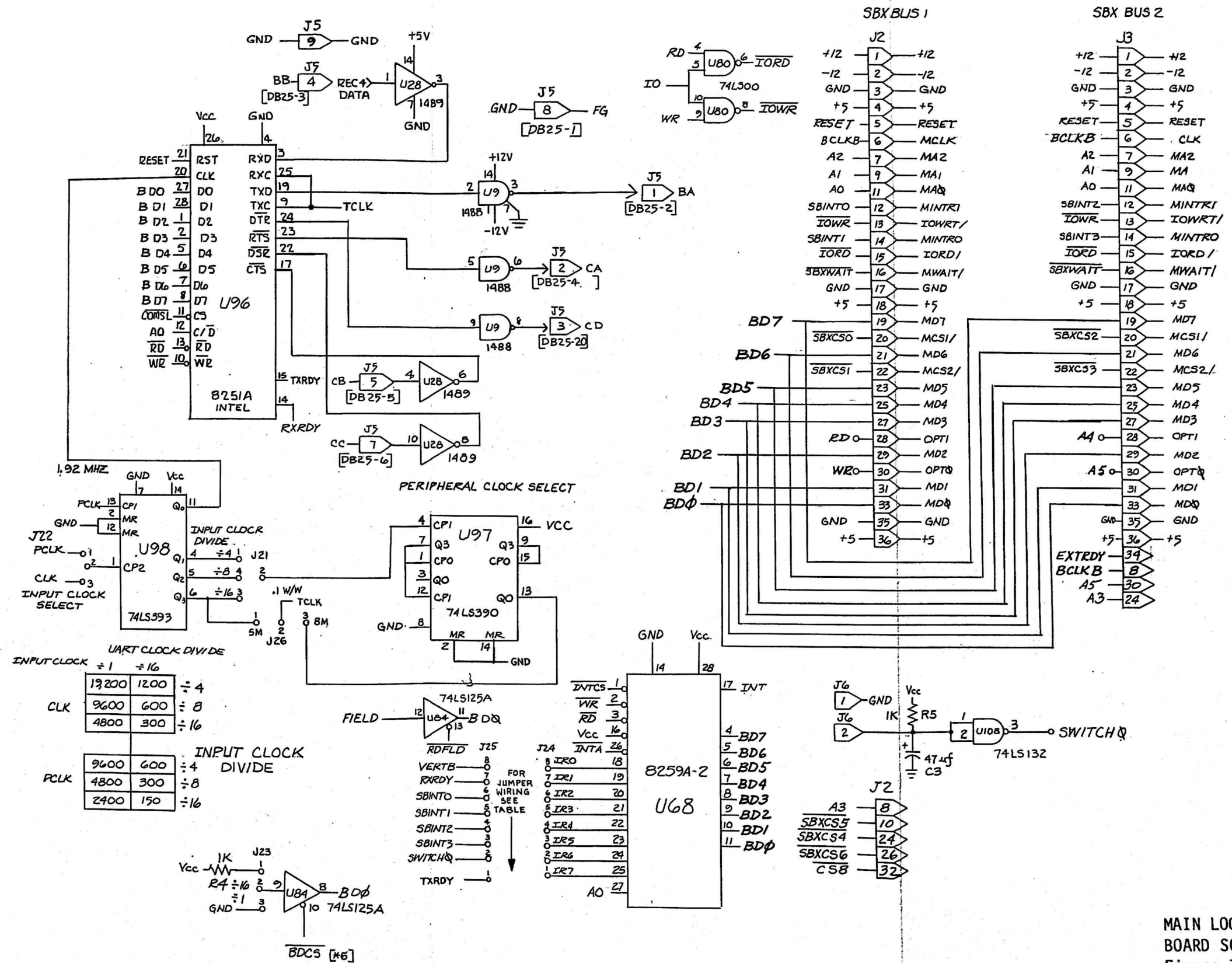
MAIN LOGIC P.C.
BOARD SCHEMATICS
Figure 7-3
Sheet 3 of 7

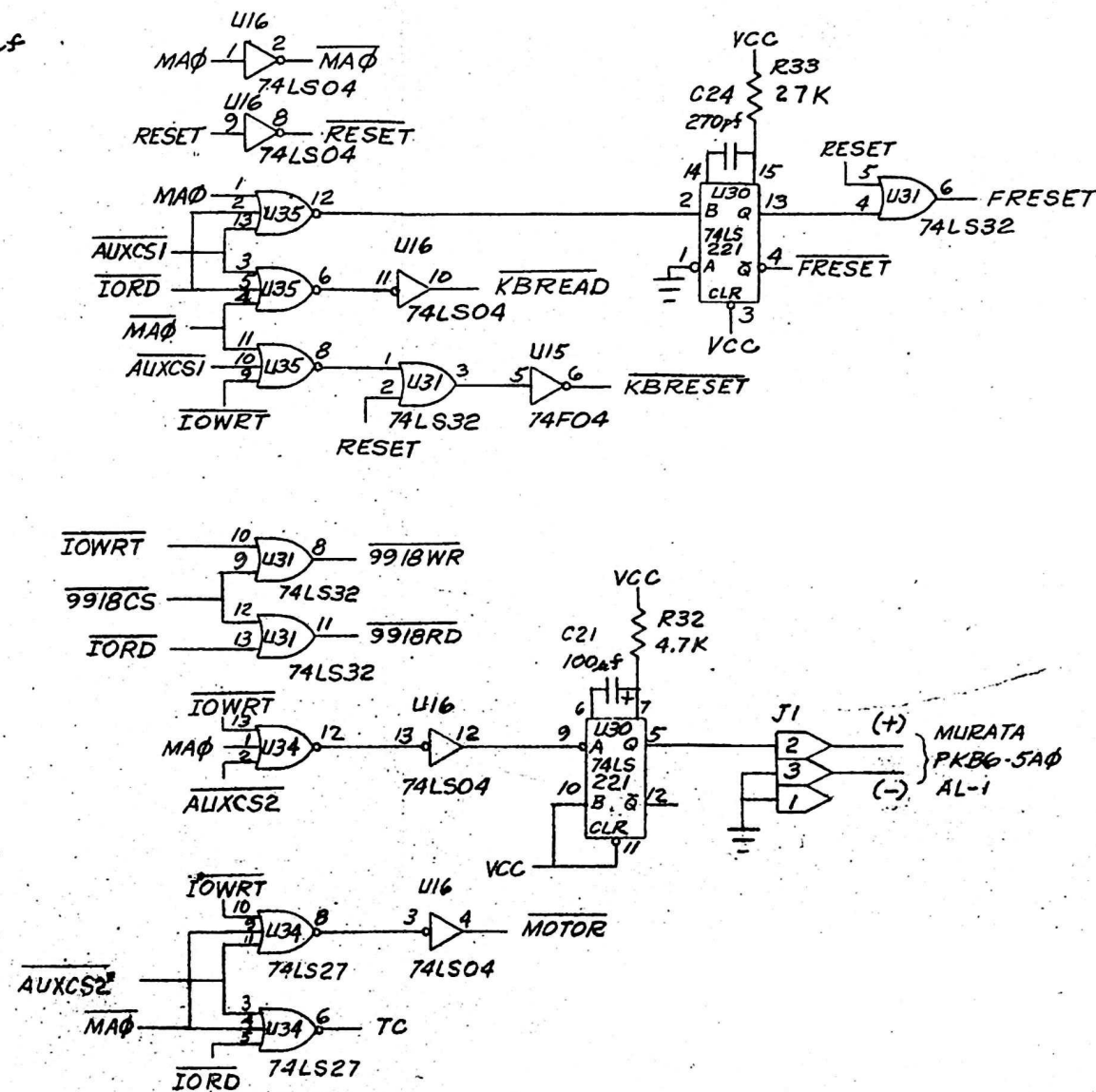
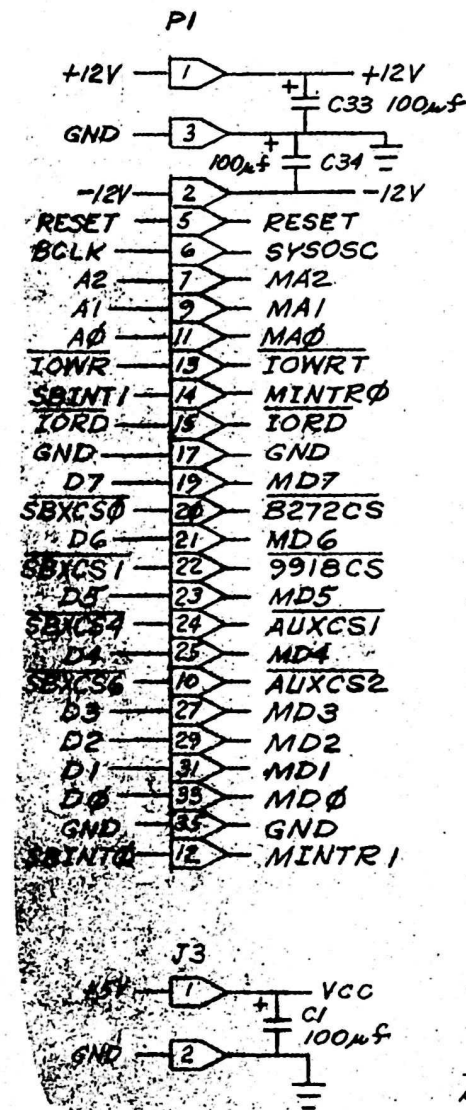
INPUT
CPU DATA BUS



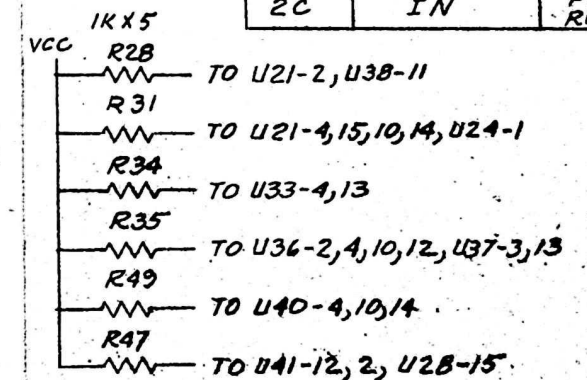
NOTE: ALL I.C.'S WITH THE SYMBOL Δ ARE
(HITACHI) NO. HM-6167-H.







PORT	DIRECTION	FUNCTION
2E	OUT	ALARM
24,25	I/O	FDC
2F	IN	FDC TC
2F	OUT	MOTOR ON/OFF 1=ON/0=OFF
2D	IN	KB READ
2D	OUT	FB CLEAR
2C	IN	FLOPPY RESET



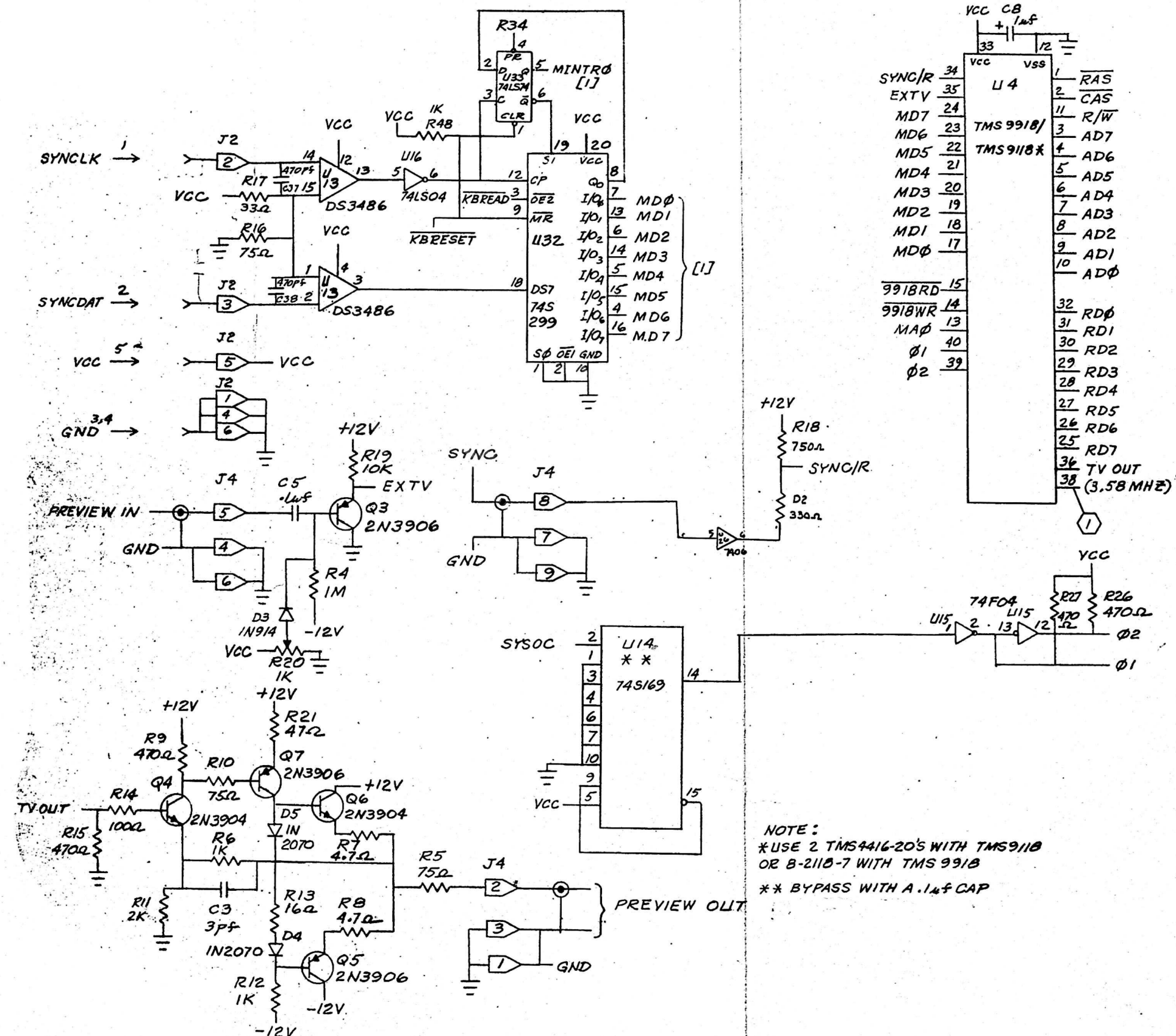
SPARE GATES

U6	DS3486	5, 6, 7, 19, 10, 11
U19	74FO4	8, 9, 10, 11, 15, 16
U23	74LS14	12, 13, 10, 11
U24	7406	12, 13, 10, 11, 8, 9
U25	74LS139	9-15
U41	74LS124	

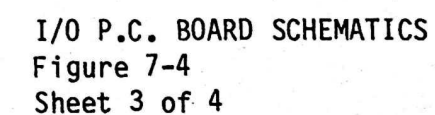
BY PASS CAPACITORS

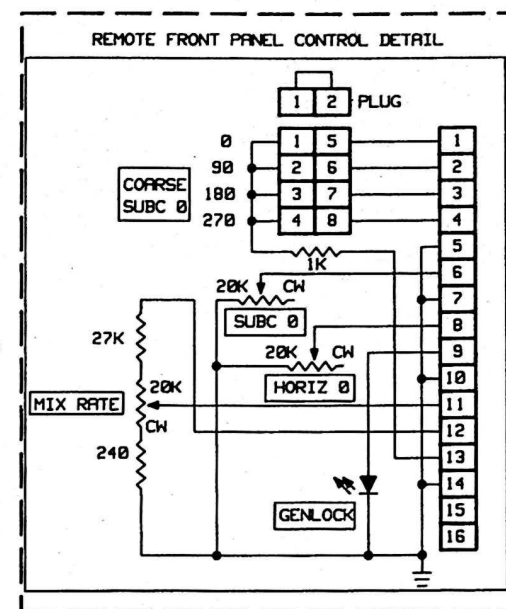
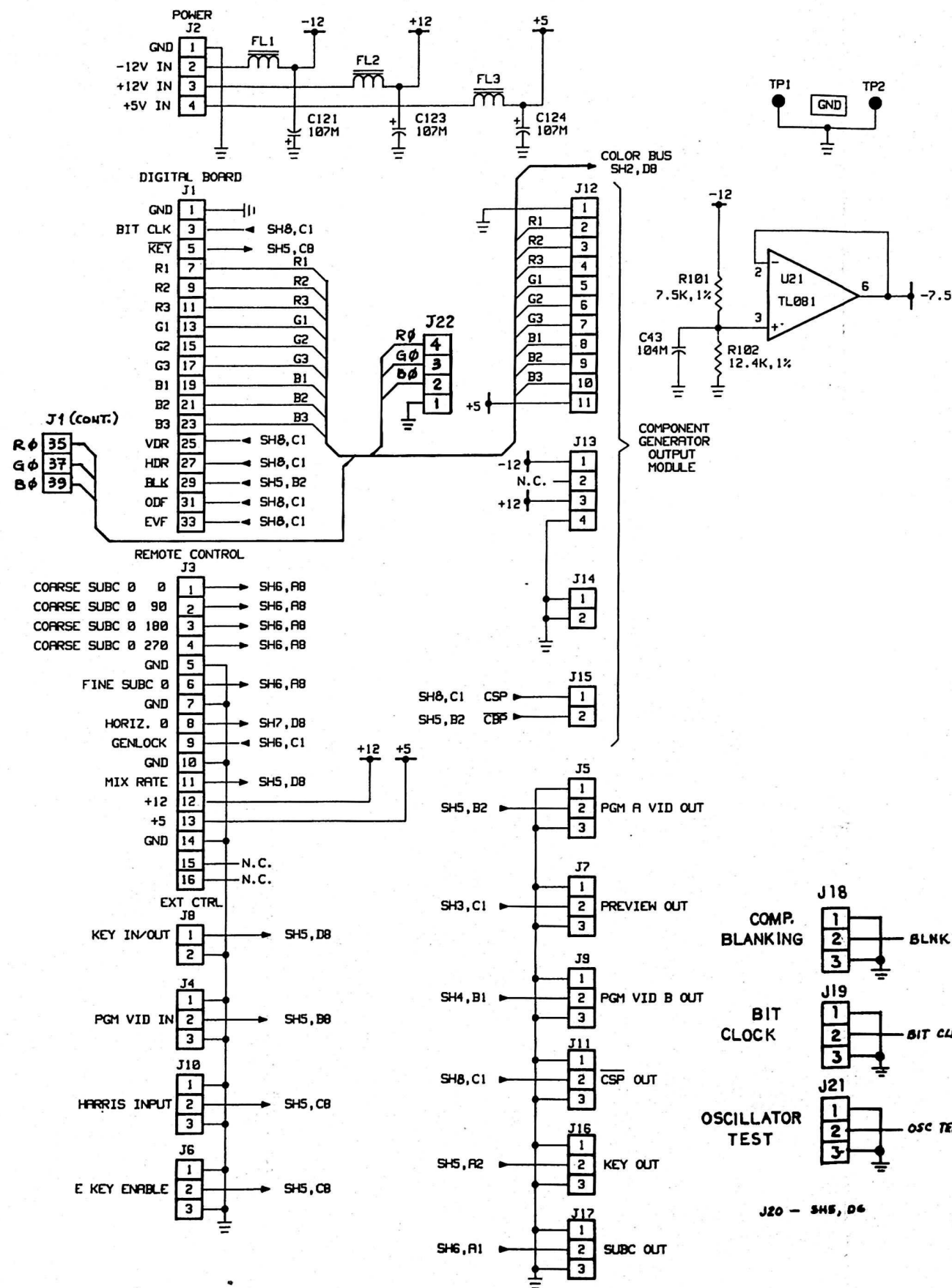
C2, C4-C7, C9-C17, C20, C22, C23, C28, C31, C32, C36 } .1μf

C27, C30, C18, C19 = .01μf



NOTE:
 *USE 2 TMS4416-20'S WITH TMS9918
 OR B-211B-7 WITH TMS 991B
 ** BYPASS WITH A .1μF CAP





- NOTES: UNLESS OTHERWISE SPECIFIED
1. RESISTOR VALUES ARE IN OHMS, 1/4W, 5%.
 2. CAPACITOR VALUES ARE IN PICOFARADS, EIA CODE
J=5% K=10% M=20%
 3. NPN TRANSISTORS ARE 2N4124
 4. PNP TRANSISTORS ARE 2N4126
 5. DIODES ARE 1N4148

I.C. POWER CONNECTIONS

TYPE	GND	+5	+12	-12
1496				14
3054	*			
3080			7	4
3086	*			
3094			7, 8	4
3140			7	4
4046				
4066	7	14		
5618	9	1		4
74HC00	7	14		
74HC02	7	14		
74HC04	7	14		
74HC32	7	14		
74HC74	7	14		
74HC86	7	14		
74HC112	8	16		
74HC164	7	14		
74HC193	8	16		
74HC221	8	16		
74HC244	10	20		
74HC374	10	20		
74LS221	8	16		
74LS624	7	9		
82S147A	10	20		
PAL10L8	9	18		
TBP28L22	10	20		
TL060	*			
TL081			7	4
TL082			8	4
74HC132	7	14		
4KX8 PROM	12	24		

*SEE SCHEMATIC

DECOUPLING CAPACITORS

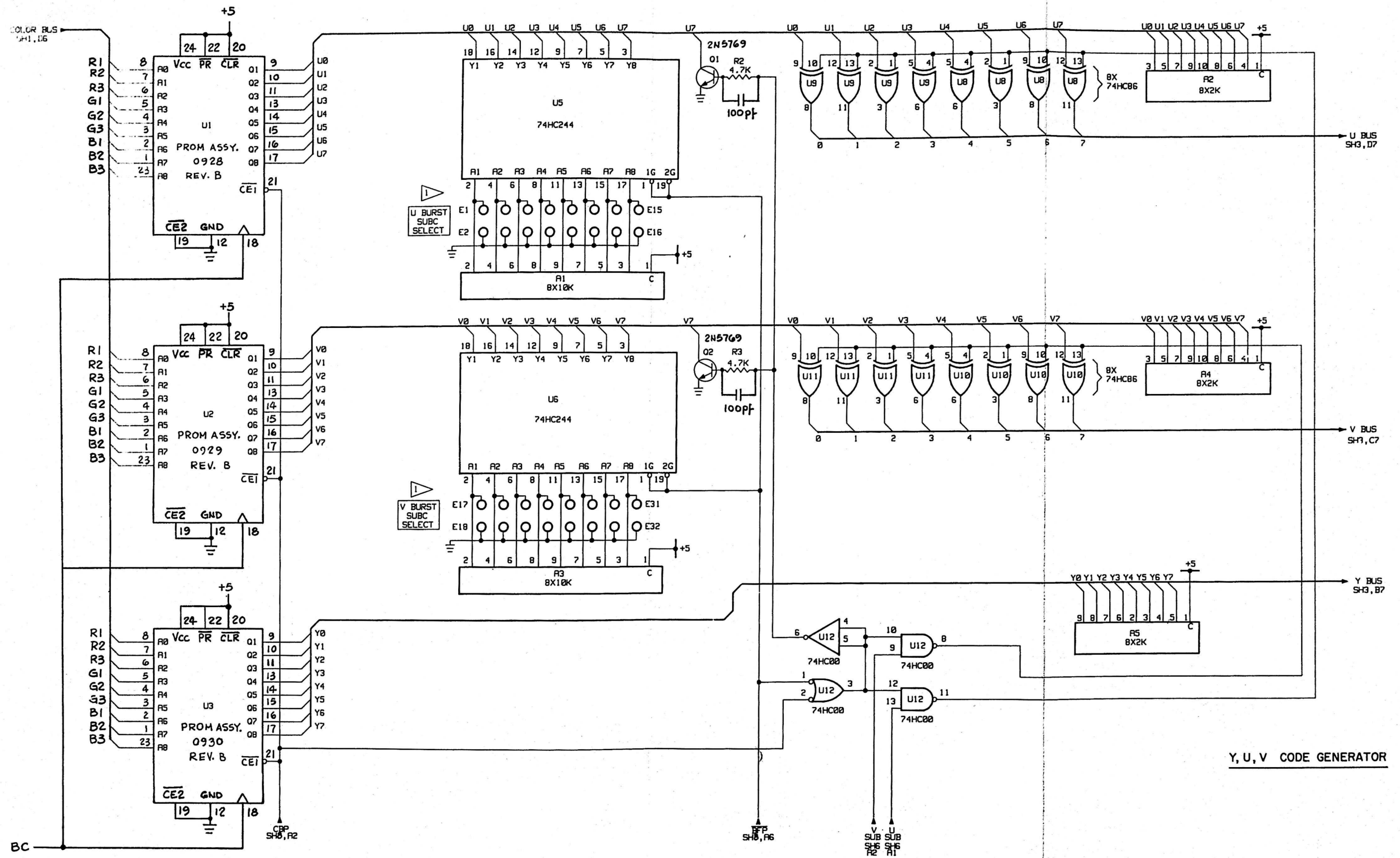
- +5
C1, 2, 4, 5, 6, 8, 9, 10, 11, 17, 40, 44, 70, 75, 80, 81, 99, 104, 106, 108, 110, 112, 113, 114, 115, 116, 117, 118, 120, 127, 128, 129, 130, 135
- +12
C13, 14, 19, 26, 27, 31, 34, 37, 38, 39, 48, 49, 55, 63, 71, 88, 90, 102, 122, 134
- 12
C12, 16, 18, 24, 30, 35, 41, 42, 45, 46, 47, 50, 58, 72, 86, 89, 132

LAST USED

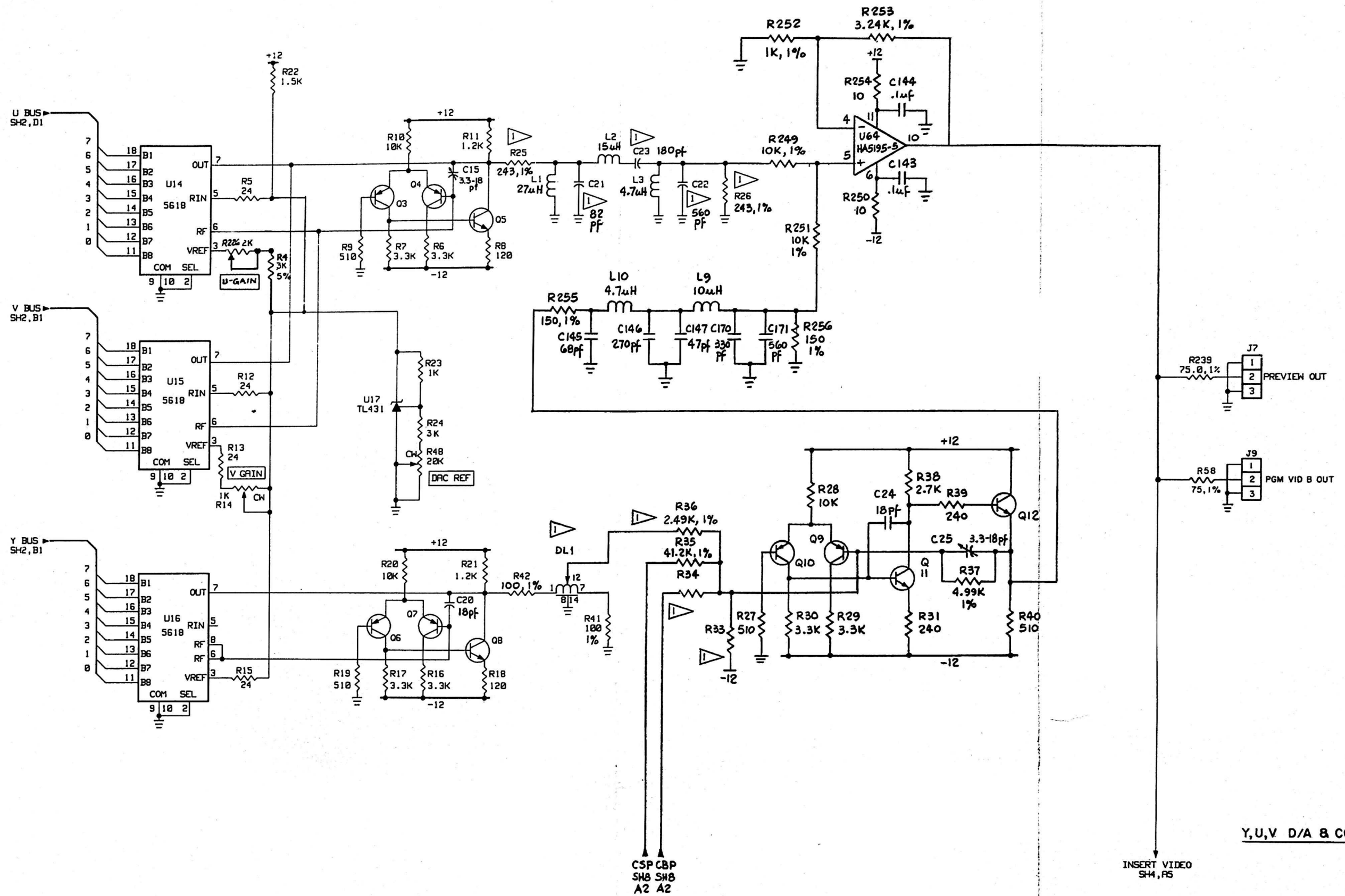
- C142
R249
044
FL3
J21
U64
L8
E62
Y1
R5
K1
DL1
CR9

REF #	NTSC	PAL	PAL-M
Y1 (MHz)	14318180	17734475	14302446
E52-E54		X	X
E55-E57		X	X
U44	0.420-0	0.430-0	0.500-0
U52	0.430-0	0.440-0	0.430-0
U59	0.431-0	0.441-0	0.431-0
R25	200	240	200
R26	200	240	200
R33	40.2K, 1%	43.2K, 1%	40.2K, 1%
R34	232K, 1%	DEL	232K, 1%
R156	47	6.8K	6.8K
R164	15K	1K	1K
R36	2.49K, 1%	2.2K, 2%	2.49K, 1%
E1-E2		X	X
E3-E4		X	X
E5-E6	X		
E7-E8		X	X
E9-E10	X	X	X
E11-E12		X	X
E13-E14	X		
E15-E16	X	X	X
E17-E18		X	X
E19-E20			
E21-E22		X	X
E23-E24			
E25-E26		X	X
E27-E28			
E29-E30		X	X
E31-E32	X		
E33-E34	X		
E35-E36	X		
E37-E38		X	X
E39-E40	X		
E41-E51	X		
E41-E42		X	X

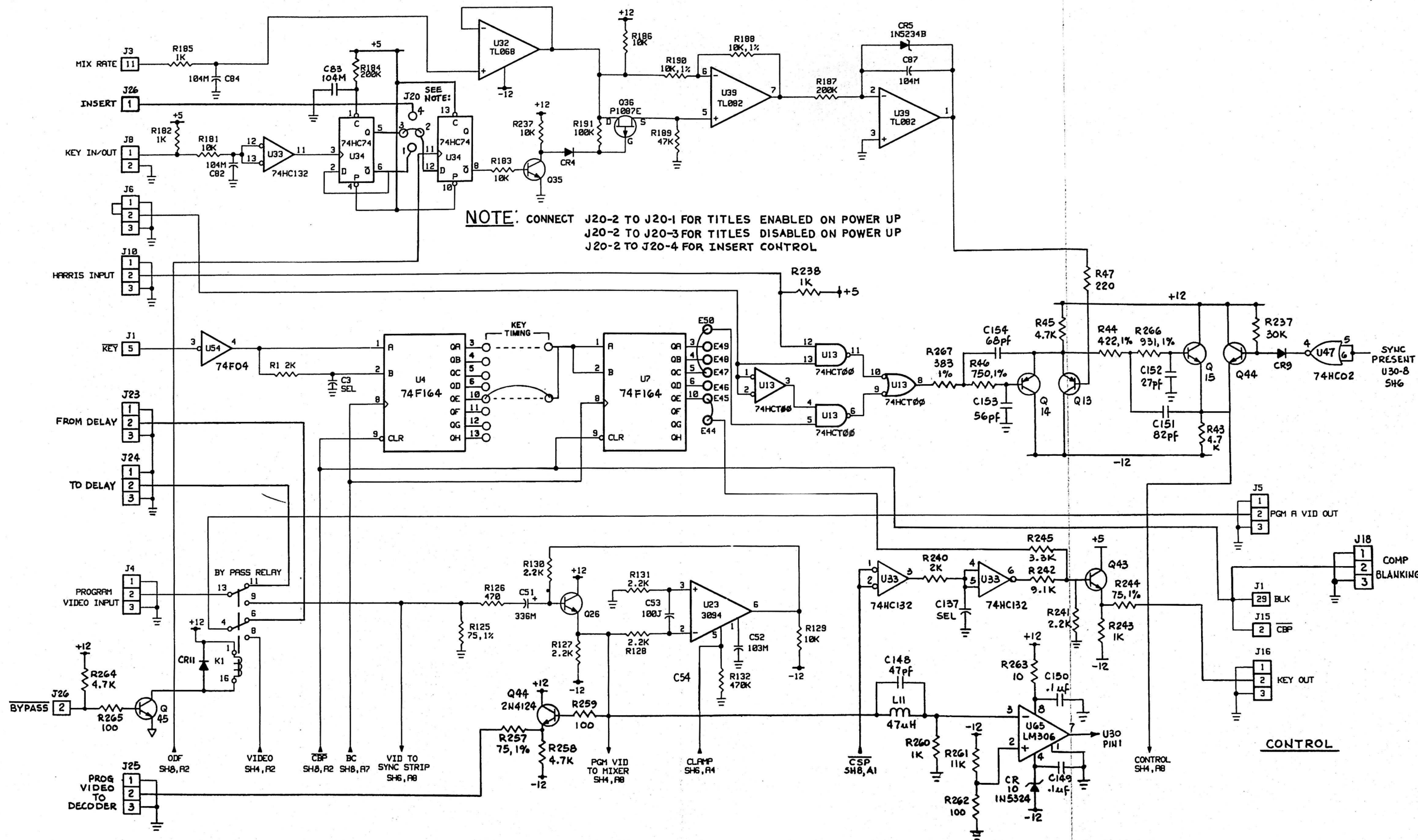
X = JUMPER



Y, U, V CODE GENERATOR



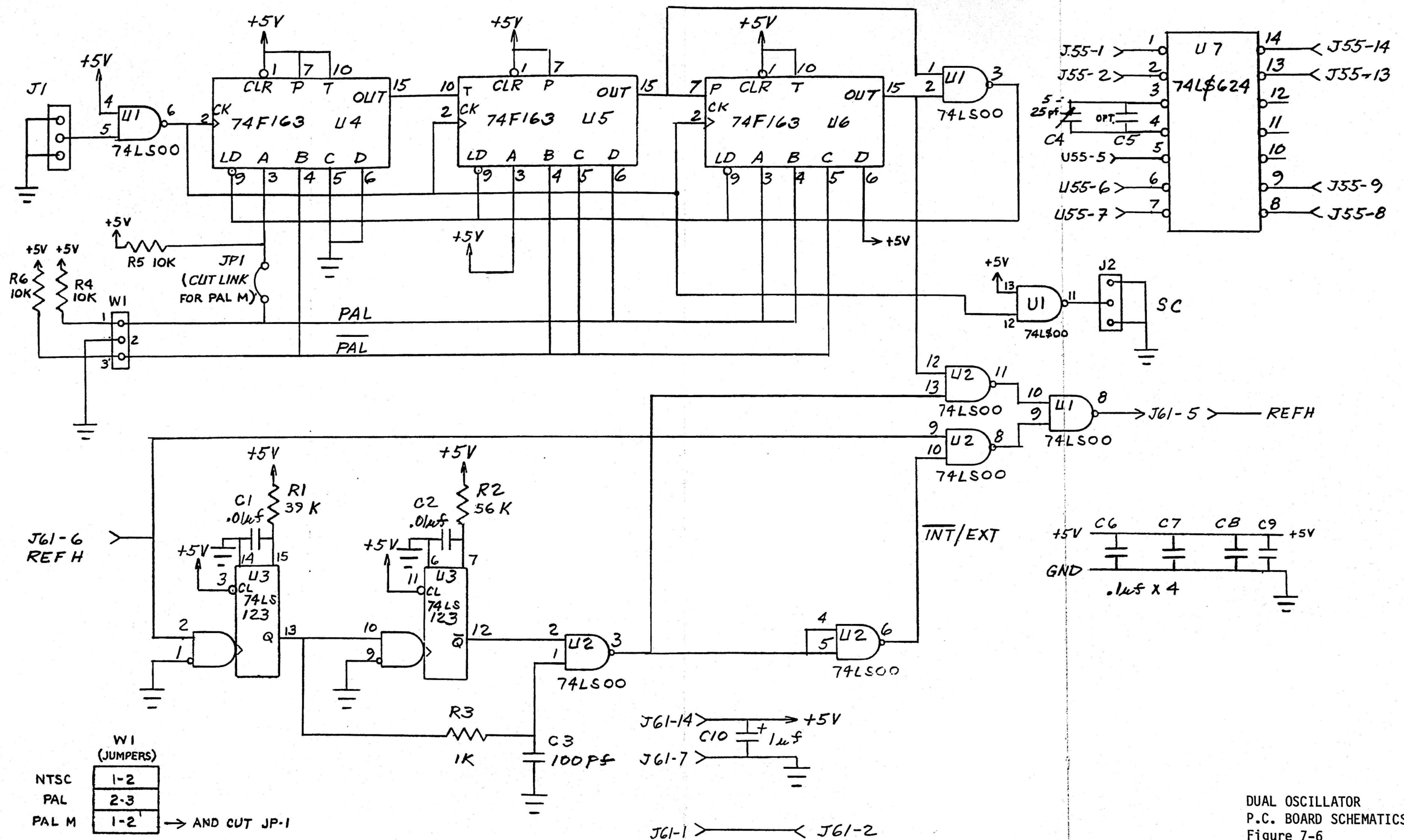
SYNC GEN/ENCODER P.C.
BOARD SCHEMATICS
Figure 7-5
Sheet 3 of 8



SYNC GEN/ENCODER P.C.
 BOARD SCHEMATICS
 Figure 7-5
 Sheet 5 of 8

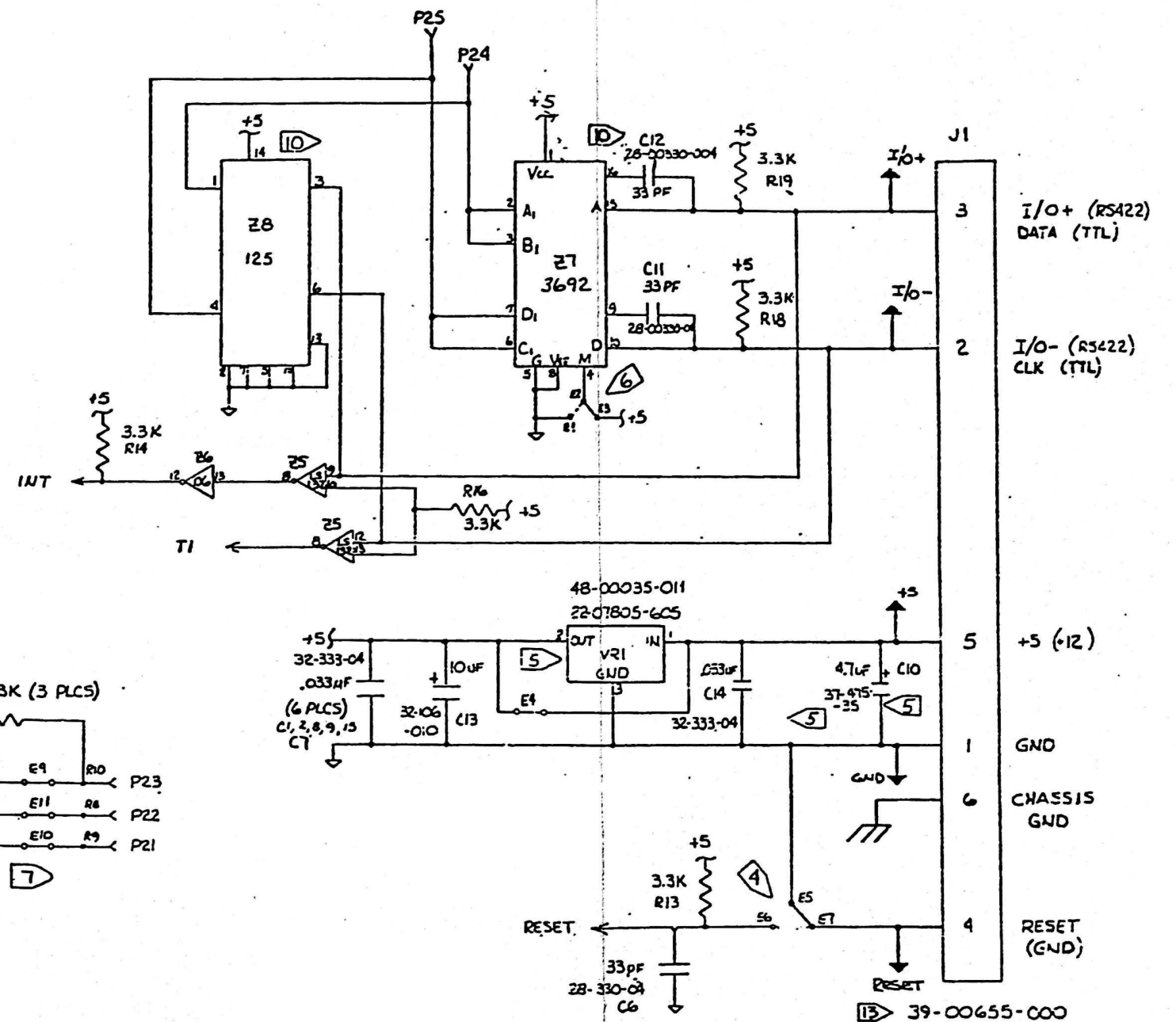
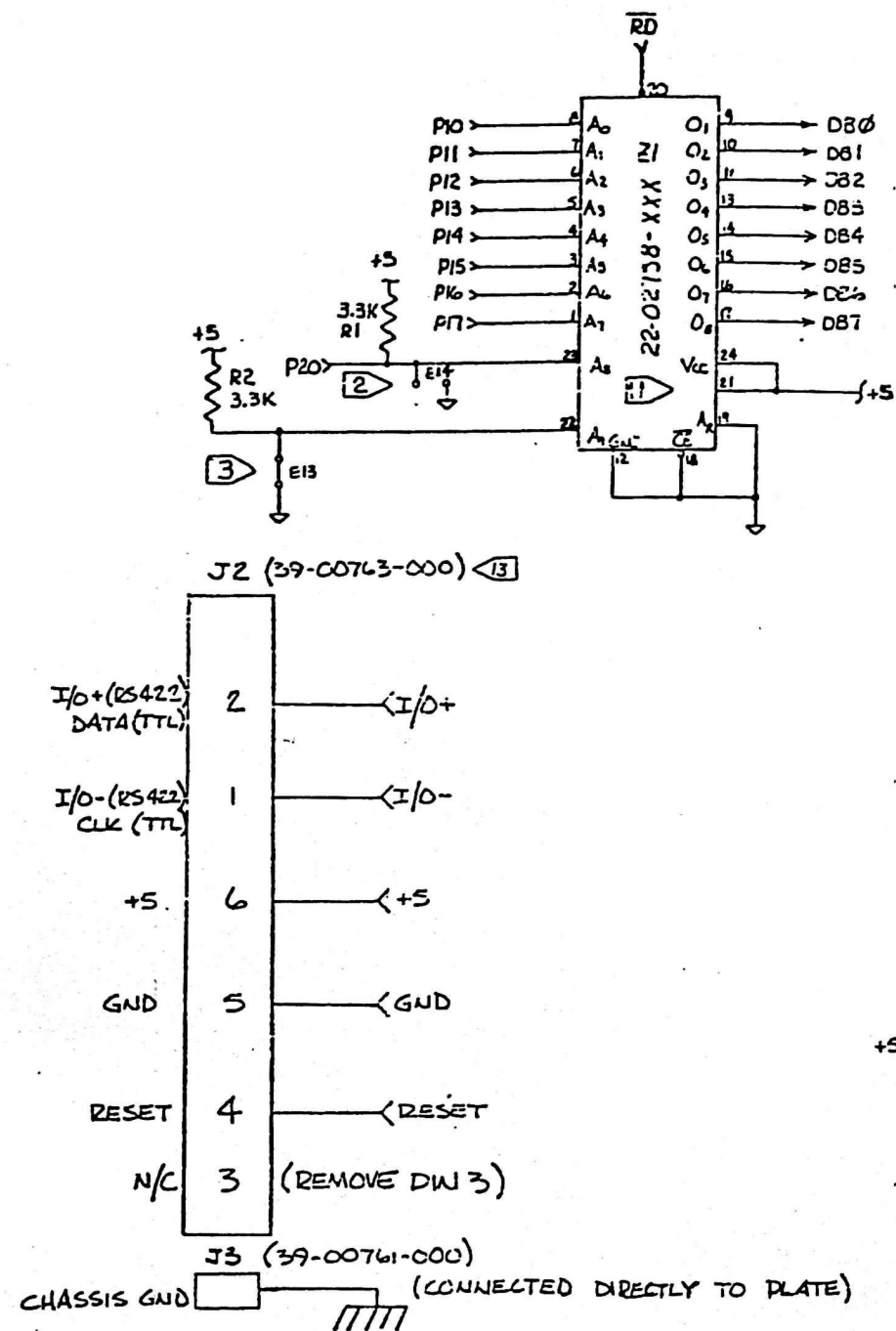


SYNC GEN/ENCODER P.C.
BOARD SCHEMATICS
Figure 7-5
Sheet 8 of 8



DUAL OSCILLATOR
P.C. BOARD SCHEMATICS
Figure 7-6
Sheet 1 of 1

Change 1



APPENDIX

TECHNICAL DATA FOR SHUGART SA300 DISK DRIVE

P/N 39254-2

SECTION II ELECTRICAL INTERFACE

2.1 INTRODUCTION

The interface of the SA300 can be divided into two categories:

- a. Signal Lines
- b. Power Lines

The following paragraphs provide the electrical definition for each line. See figure 2-1 for all interface connections.

2.2 SIGNAL INTERFACE

The signal interface consists of two categories:

- a. Control Lines
- b. Data Transfer Lines

All lines in the signal interface are digital in nature and provide signals to the drive (input) or to the host (output) via interface connector P1/J1.

2.2.1 Input Lines

The input signals are of three types: those intended to be multiplexed in a multiple drive system, those which will perform the multiplexing, and those signals which are not multiplexed and affect all the drives in a daisy chain system.

The input signals to be multiplexed are:

- a. DIRECTION SELECT
- b. STEP
- c. WRITE DATA
- d. WRITE GATE

The input signals which are intended to do the multiplexing are:

- a. DRIVE SELECT 1
- b. DRIVE SELECT 2
- c. DRIVE SELECT 3
- d. DRIVE SELECT 4

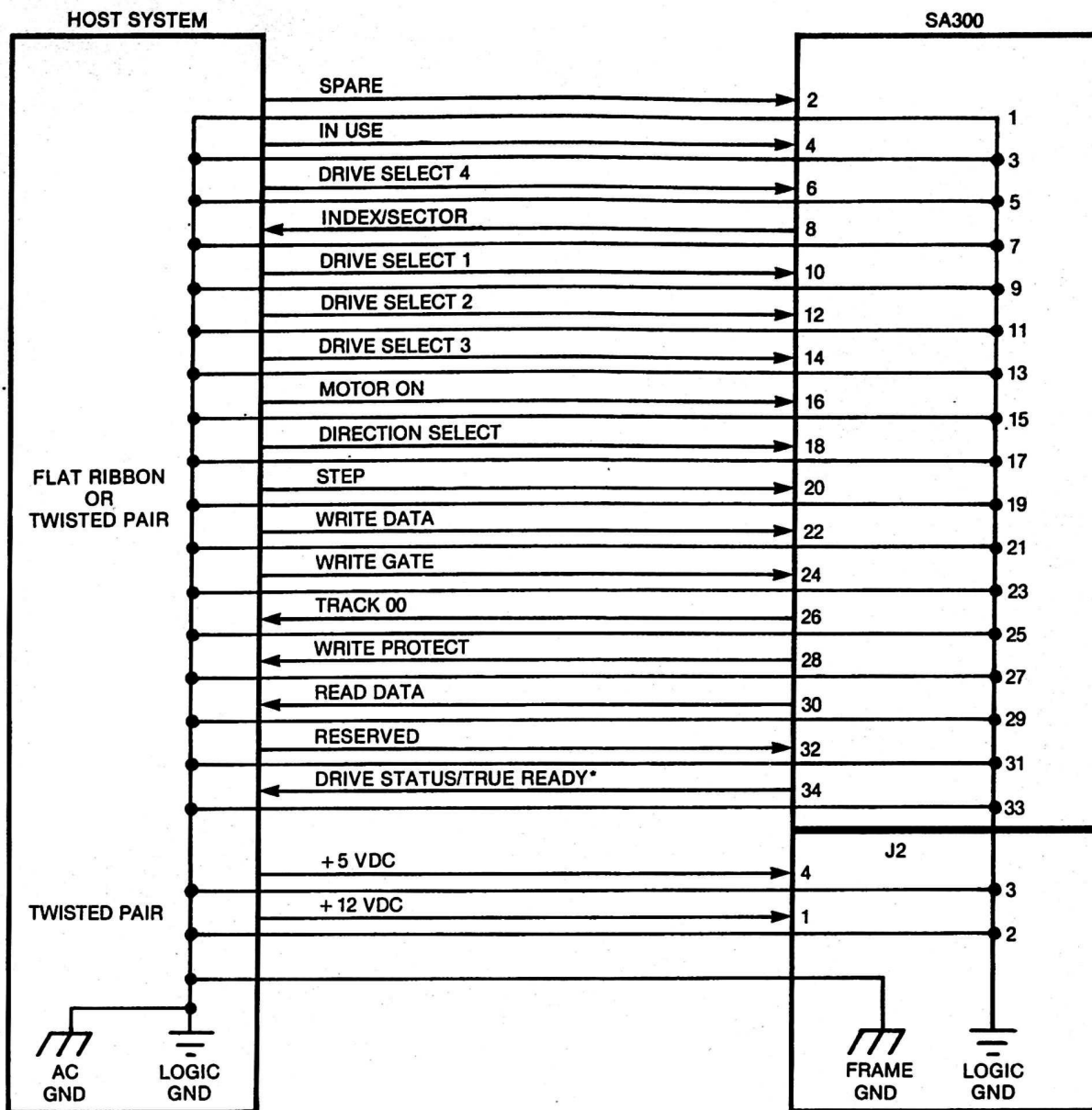
The signals which are not multiplexed are IN USE and MOTOR ON.

The input lines have the following electrical specifications. See figure 2-2 for the recommended circuit.

True = Logical zero = $V_{in} + 0.0$ to $+0.04$ V @ 40 mA (max)

False = Logical one = $V_{in} + 2.5$ to $+5.25$ V @ 250 μ A (open)

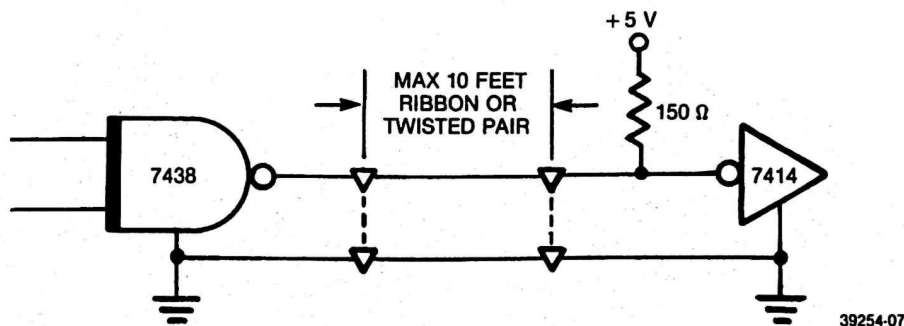
Input impedance = 150 ohms



*TRUE READY IS A CUSTOMER JUMPER OPTION

39254-06

FIGURE 2-1. INTERFACE CONNECTIONS



39254-07

FIGURE 2-2. INTERFACE SIGNAL DRIVER/RECEIVER

2.2.2 Input Line Terminations

The SA300 has been provided with the capability of terminating the six input lines listed below.

- a. MOTOR ON
- b. DIRECTION SELECT
- c. STEP
- d. WRITE DATA
- e. WRITE GATE
- f. IN USE

These lines are terminated through a 150 ohm resistor pack installed in a SIP socket.

In a single drive system, this resistor pack should be kept in place to provide the proper terminations.

In a multiple drive system, only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed. External terminations may also be used. However, the user must provide the terminations beyond the last drive and each of the six lines must be terminated to +5 V dc through a 222/330 ohm, 1/4 watt resistor, or a 150 ohm, 1/4 watt resistor.

2.2.3 Drive Select 1-4

The SA300 is configured to operate with up to four drives in a multiplexed multiple drive system.

SINGLE DRIVE SYSTEM (MX shorting plug installed)

With MX shorted, the I/O lines are always enabled.

MULTIPLE DRIVE SYSTEM (MX shorting plug not installed)

Four separate input lines (DRIVE SELECT 1 through DRIVE SELECT 4) are provided so that up to four drives in a multiplexed system may have separate input pins. Only the drive with its unique DRIVE SELECT line active will allow the drive to respond to multiplexed input lines, and enable the outputs to drive their respective signal lines. A logical zero on the interface selects a unique drive select line for a drive. With the MS shorting plug installed, DRIVE SELECT (when activated to a logical zero level) will turn the motor on.

2.2.4 Motor On

This input, when activated to a logical zero level, will turn on the drive motor allowing reading or writing on the drive. A 0.5 second delay after activating this line must be allowed before reading or writing. For maximum motor life, this line should be deactivated if no commands have been issued to the drive within two seconds (10 revolutions of the media) after completion of a previous command. This time may be varied by the host system to maximize system through-put and motor life, depending on the application.

As discussed in paragraph 2.2.3, when MS is shorted, the motor will turn on if either the DRIVE SELECT line or the MOTOR ON line is activated. A user selectable option is available that allows the motor to turn on only when the MOTOR ON line is activated.

2.2.5 Direction Select

This interface line defines the direction of motion the read/write heads will take when the STEP line is pulsed. An open circuit, or logical one, defines the direction as "out." If a pulse is applied to the STEP line, the read/write heads will move away from the center of the disk. Conversely, if this input is shorted to ground or a logical zero level, the direction of motion is defined as "in." If a pulse is applied to the STEP line, the read/write heads will move towards the center of the disk.

2.2.6 Step

This interface line is a control signal which causes the read/write heads to move in the direction of motion defined by the DIRECTION SELECT line. This signal must be a logical zero going pulse with a minimum pulse width of $1\ \mu\text{s}$ and a logical one for 5.5 ms minimum between adjacent pulses. Each subsequent pulse must be delayed by 6 ms minimum from the preceding pulse for normal mode or $50\ \mu\text{sec}$ in buffered step mode. Refer to Section 1.4.5 for buffered seek operation.

The access motion is initiated on each logical zero to logical one transition, or at the trailing edge of the signal pulse. Any change in the DIRECTION SELECT line must be made at least $1\ \mu\text{s}$ before the trailing edge of the step pulse, the DIRECTION SELECT logic level must be maintained $1\ \mu\text{s}$ after the trailing edge of the step pulse. See figure 2-3 for these timings.

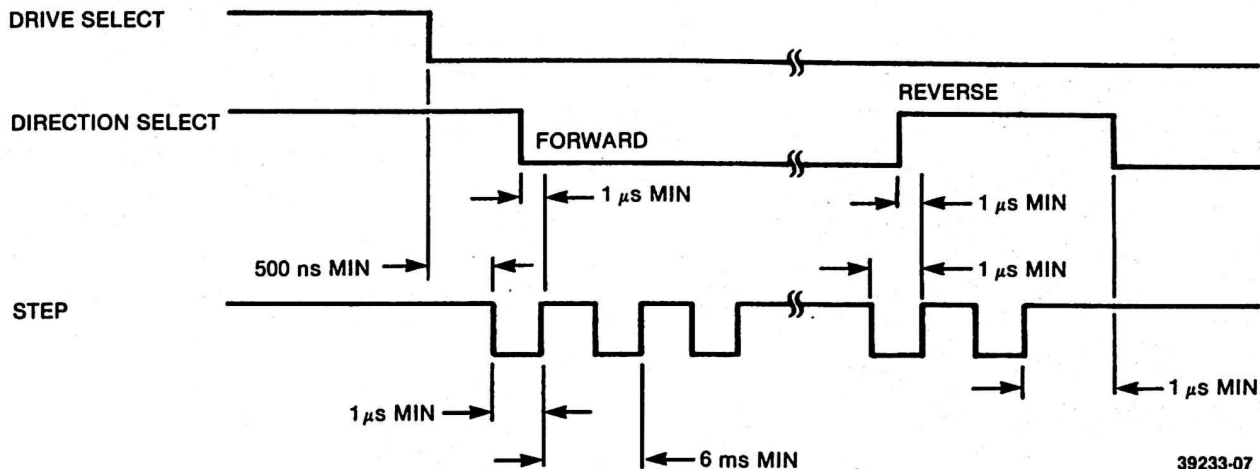


FIGURE 2-3. STEP TIMING

2.2.7 Write Gate

The active state of this signal, or logical zero, enables write data to be written on the diskette. The inactive state, or logical one, enables the read data logic and stepper logic. See figure 1-7 for timings.

2.2.8 Write Data

This interface line provides the data to be written on the diskette. Each transition from a logical one level to a logical zero level will cause the current through the read/write head to be reversed thereby writing a data bit. This line is enabled by WRITE GATE being active. WRITE DATA must be inactive during a read operation. See figure 1-8 for timings.

2.2.9 In Use

Normally, the activity LED on the selected drive will turn on when the corresponding DRIVE SELECT signal is active. The IN USE input can alternately activate the LED on all drives in a daisy chain or separately in a radial configuration.

2.2.10 Output Lines

The output control lines have the following electrical specifications. See figure 2-2 for the recommended circuit.

True = Logical zero = $V_{\text{out}} + 0.0$ to $+0.4\ \text{V}$ @ $40\ \text{mA}$ (max)

False = Logical one = $V_{\text{out}} + 2.5$ to $+5.25\ \text{V}$ (open collector) @ $I = 250\ \mu\text{A}$ (max)

2.2.11 Track 00

The active or logical zero state of this interface signal indicates when the read/write head of the drive is positioned at track zero (the outermost track) and the stepper is locked on track. This signal is at a logical one level, or inactive state, when the read/write head is not at track 00. When the read/write head is at track 00 and an additional step out pulse is issued to the drive, microprocessor logic will keep the read/write head positioned at track 00.

2.2.12 Index

This interface signal is provided by the drive each motor revolution. Normally, this signal is at a logical one level and makes the transition to the logical zero level each revolution of the spindle motor.

There is one pulse on this interface signal per revolution of the-diskette (200 ms). This pulse indicates the physical beginning of a track. See figure 2-4 for timings.

When using the INDEX signal, look for an edge or transition rather than a level for determining the status.

2.2.13 Read Data

This interface line provides the "raw data" (clock and data together) as detected by the drive electronics. Normally, this signal is a logical one level and becomes a logical zero level for the active state. See figure 1-5 for the timing and bit shift tolerance within normal media variations.

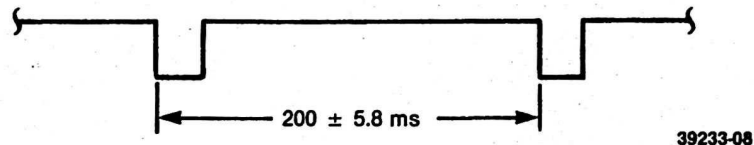


FIGURE 2-4. INDEX TIMING (SA130-SOFT SECTORED MEDIA)

2.2.14 Write Protect

This interface signal is provided by the drive to indicate to the user that a write protected cartridge is installed. The signal is logical zero level when it is protected. The drive will inhibit writing with a protected diskette installed and, additionally, notifies the interface.

2.2.15 Drive Status

This interface line provides information on the status of the drive. The information relayed is determined by whether the TR jumper is open or shorted and whether or not TP 11 is shorted to TP 10 (gnd).

TR Shorted, TP 11 Open (Disk In), Normal Configuration as Shipped

The DRIVE STATUS line goes to the active (logical zero) level when a cartridge is inserted in the drive.

TR Open, TP 11 Open (TRUE READY)

The line goes to the active (logical zero) level when **all** of the following conditions are met:

- a. The cartridge is inserted in the drive.
- b. The spindle motor is on and up to speed.
- c. The head is settled on the specified data track.

TR Open, TP 11 Grounded (Disk Change)

The line goes to the active (logical zero) level when **all** the following conditions are met:

- a. The cartridge is in the drive.
- b. The cartridge has not been removed since the drive was last deselected.
- c. An index pulse has been sensed after conditions a) and b) were met.

If the **Drive Status** signal is inactive, the user may deselect and then select the drive to test **Drive Status** again; if the cartridge had previously been removed but is now inserted, **Drive Status** will activate upon sensing an index pulse.

This option cannot be used (i.e., **Drive Status** will never become active) when the MX jumper is shorted, because condition b) will never be met.

Figure 2-5 shows the equivalent logic of this function.

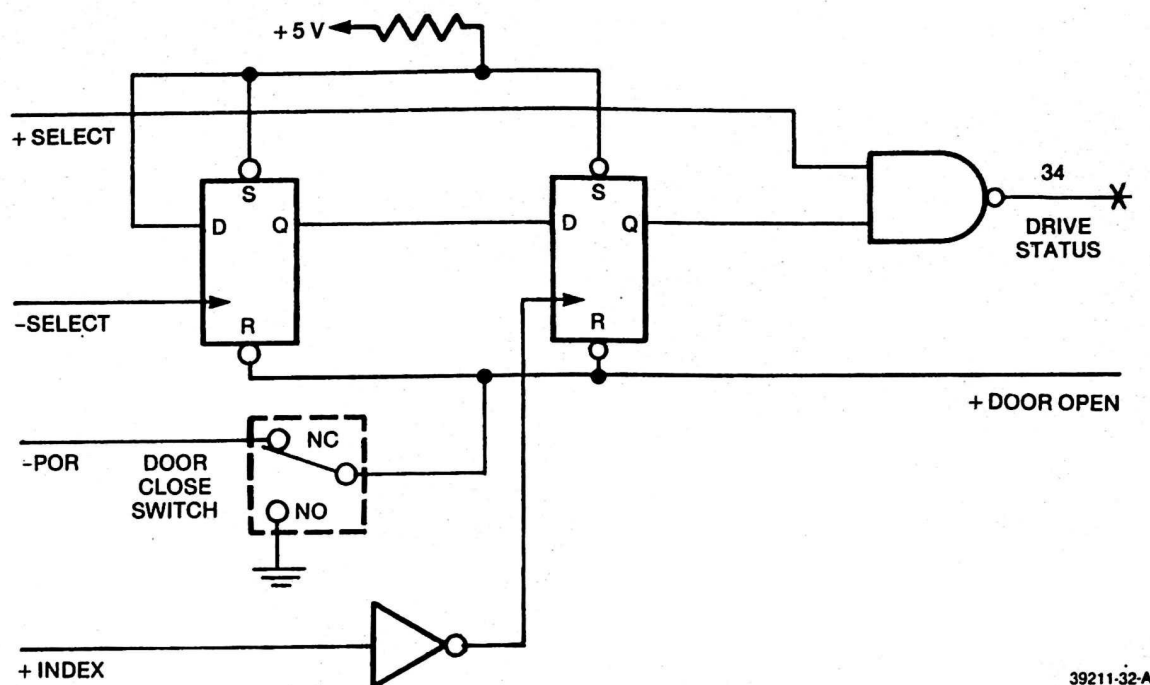


FIGURE 2-5. DISK CHANGE DRIVE STATUS LOGIC

TR Open, TP 11 Grounded (TRUE READY and Disk Change)

The line goes to the active (logical zero) level when **all** the conditions for TRUE READY and **all** the conditions for Disk Change are met as follows:

- The cartridge is in the drive.
- The spindle motor is on and up to speed.
- The head is settled on the specified data track.
- The cartridge has not been removed since the drive was last deselected.
- An index pulse has been sensed since conditions a), b), c) and d) were met.

If the **Drive Status** signal is inactive, the user may deselect and then select the drive to test **Drive Status** again; if the cartridge had previously been removed but is now inserted, **Drive Status** will activate upon sensing an index pulse after the spindle motor is up to speed.

This option cannot be used (i.e., **Drive Status** will never become active) when the MX jumper is shorted, because condition "d" will never be met.

2.2.16 Self Test

If TP 9 is grounded when power is first applied to the drive, a self test will be performed before the drive responds to the interface. If the drive is functioning properly, the activity LED will flash for approximately 8 seconds following a 2 second initial delay when it will be OFF. If the drive should fail the self test, the LED will remain at a steady level (On or Off) for 12 seconds. Following the completion of the self test sequence and display the drive will begin to service the interface normally.

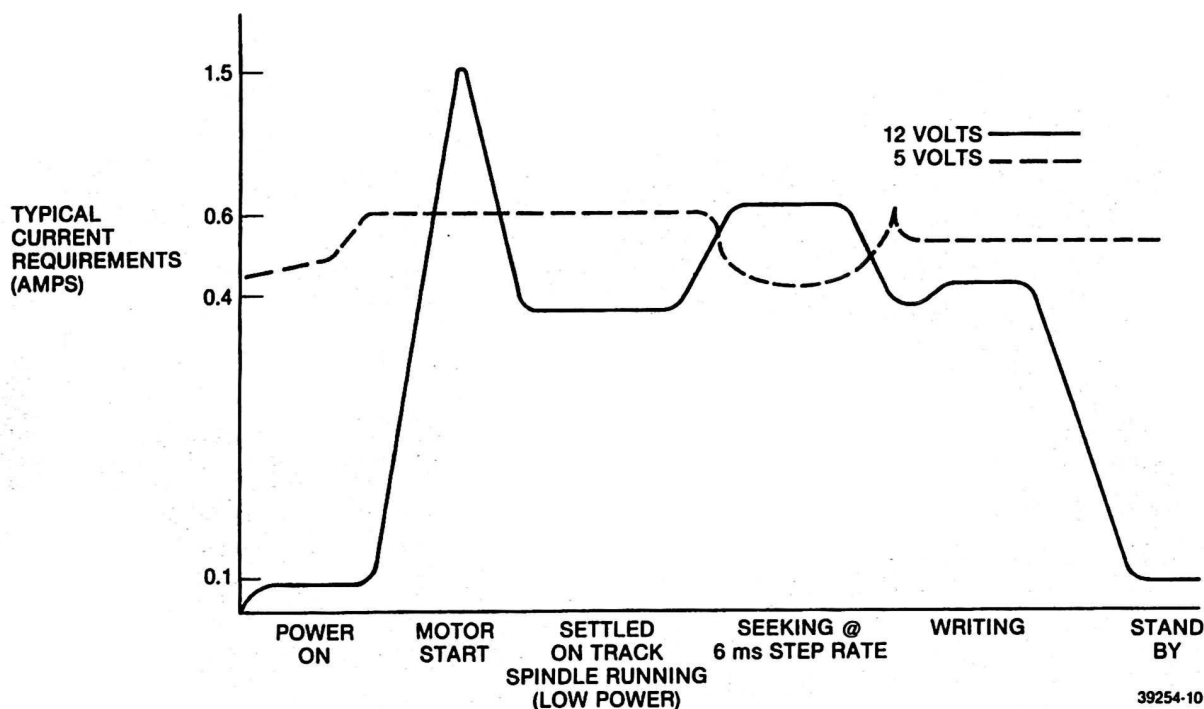
TP 9 need only be grounded for 1 second after power is applied to initiate the self test; if TP 9 is shorted to ground (TP 10), the self test will be executed each time the power is applied. A cartridge need not be in the drive and no interface signals are required to perform the self test.

The self test sequence verifies the drive's internal microprocessor and associated circuitry, stepper motor, track 0 sensor, spindle motor, index sensor and activity LED.

TABLE 2-1. DC POWER REQUIREMENTS

P2 PIN	DC VOLTAGE	TOLERANCE	CURRENT	MAX RIPPLE (p to p)
1	+ 12 VDC	± 0.6 VDC	1.5 A MAX 0.4 A TYP	100 mV MAX ALLOWABLE
2	+ 12 RETURN			
3	+ 5 RETURN			
4	+ 5 VDC	± 0.25 VDC	0.70 A MAX 0.60 A TYP	50 mV MAX ALLOWABLE

39254-09



39254-10-A

FIGURE 2-6. DC POWER PROFILE

2.3 POWER INTERFACE

The SA300 requires only dc power for operation. DC power to the drive is provided via P2/J2 located on the component side of the PCB near the spindle drive motor. The two dc voltages, their specifications and their J2/P2 pin designators are outlined in table 2-1. The specifications outlined on current requirements are for one drive. For multiple drive systems, the current requirements are a multiple of the maximum current times the number of drives in the system. Figure 2-5 illustrates the SA300 dc power profile.

2.4 FRAME GROUND

CAUTION

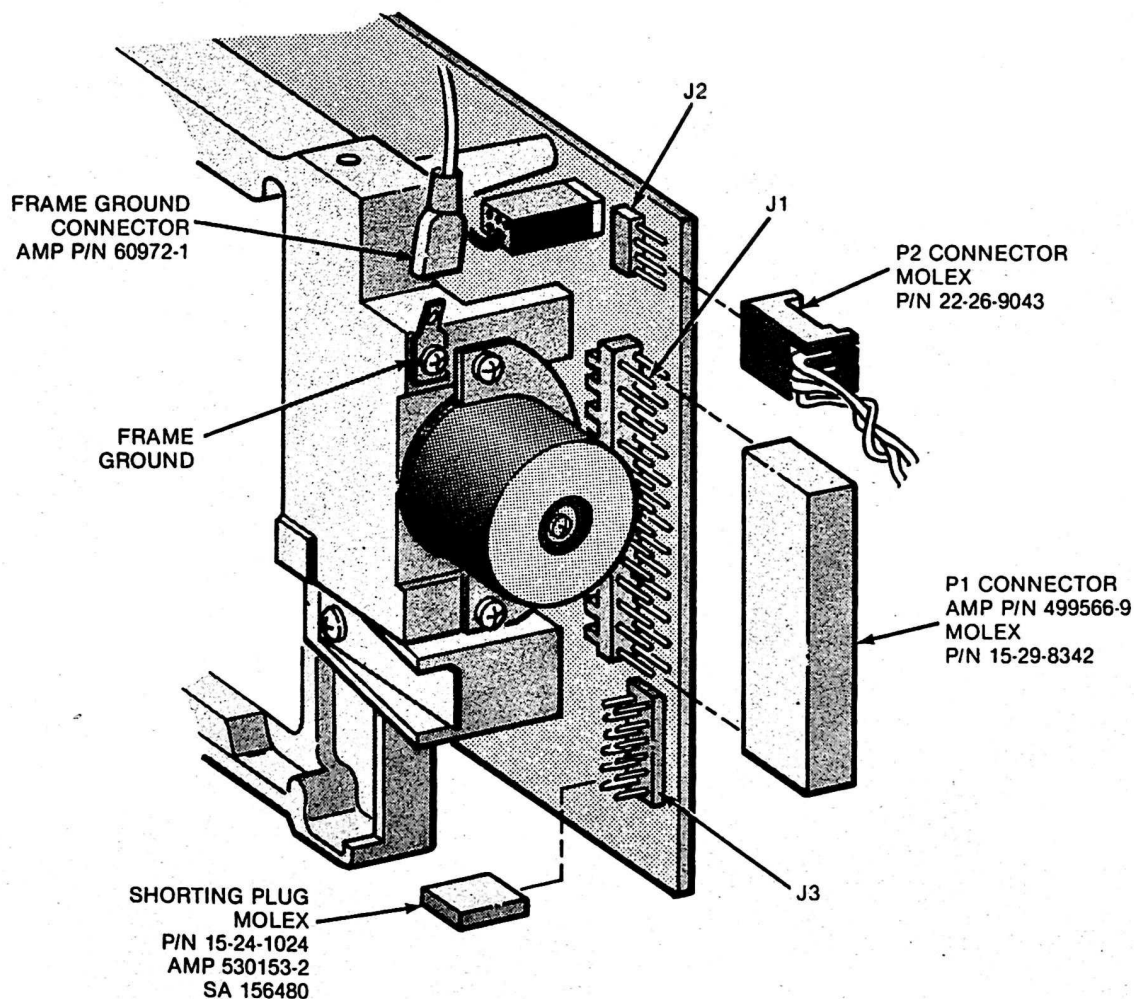
It is important that the drive be frame grounded to the ac ground or frame ground of the host system. Failure to do so may result in drive noise susceptibility. Refer to paragraph 3.3 for the procedure.

SECTION III PHYSICAL INTERFACE

3.1 INTRODUCTION

The electrical interface between the 300/350 and the host system is via two connectors. The first connector, J1, provides the signal interface and the second connector, J2, provides the dc power.

This section describes the locations of the connectors on the drive and the recommended connectors to be used with them. See figure 3-1 for connector locations.



39254-11-A

FIGURE 3-1. INTERFACE CONNECTORS — PHYSICAL LOCATIONS

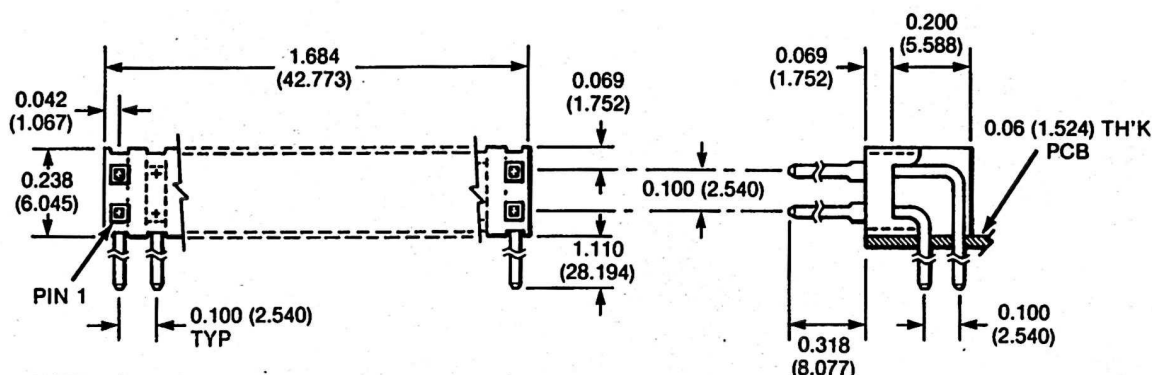
3.2 J1/P1 CONNECTOR

Connection to J1 is through a PCB pin type connector. The dimensions and location of pin 1 for the connector are shown in figure 3-2. Pins are numbered 1 through 34 with the even numbered pins on the top row. Pins 1, 2, and 34 are numbered on the PCB. Keying is not available with this connector. The recommended connectors for P1 are shown in table 3-1.

TABLE 3-1. RECOMMENDED J1 CONNECTORS

TYPE OF CABLE	MANUFACTURER	CONNECTOR P/N
FLAT CABLE	3M "SCOTCHFLEX"	AMP 499566-9

39254-24-A

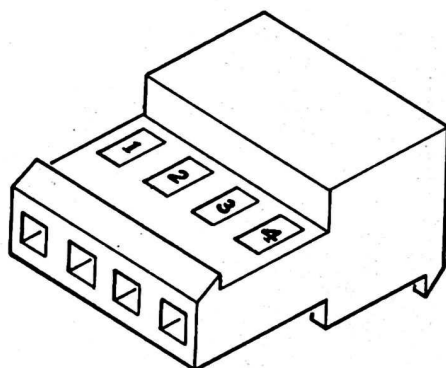


39254-25

FIGURE 3-2. J1 CONNECTOR DIMENSIONS

3.3 J2/P2 CONNECTOR

The dc power connector, J2, is mounted on the component side of the PCB and is located near the stepper motor. J2 is a 4 pin AMP data connector P/N 87232-4. The recommended mating connector and pins (P2) is Molex P/N 22-26-9043. J2, pin 1, is labeled on the component side of the PCB. Figure 3-3 illustrates the J2 connector.



P2 CONNECTOR PIN

1	+ 12 V DC
2	+ 12 RETURN
3	+ 5 RETURN
4	+ 5 V DC

39254-13

FIGURE 3-3. J2/P2 CONNECTOR

3.4 FRAME GROUNDING

The drive must be frame grounded to the host system to ensure proper operation. If the frame of the drive is not fastened directly to the frame of the host system with a good ac ground, a wire from the system ac frame ground must be connected to the drive. For this purpose, a faston tab is provided on the drive where a faston connector can be attached or soldered. The tab is AMP P/N 61664-1 and its mating connector is AMP P/N 60972-1.

SECTION IV

DRIVE PHYSICAL SPECIFICATIONS

4.1 GENERAL

This section contains the mechanical dimensions and mounting recommendations for the 300/350.

4.2 MOUNTING

NOTE

Do not mount the drive in horizontal position with PCB down.

As shipped from the factory, the drive is capable of being mounted in either of the following positions (see figure 4-1):

1. Top Loading — mounted upright.
2. Front Loading — mounted vertical with the PCB either on the left or right.
— mounted horizontal with PCB up.

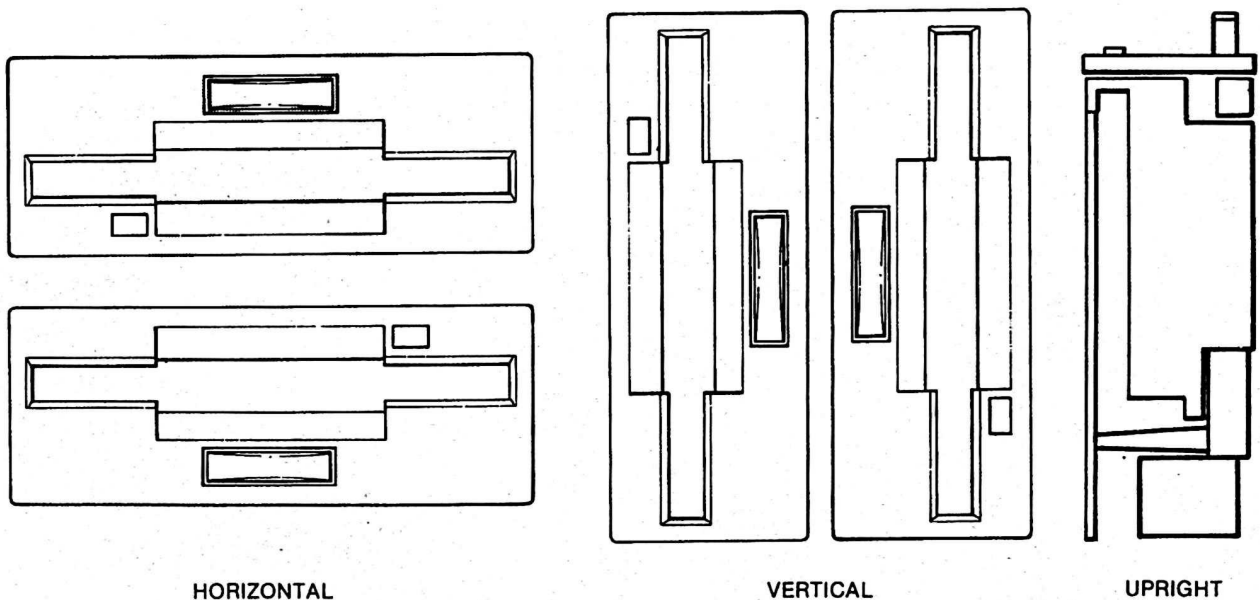
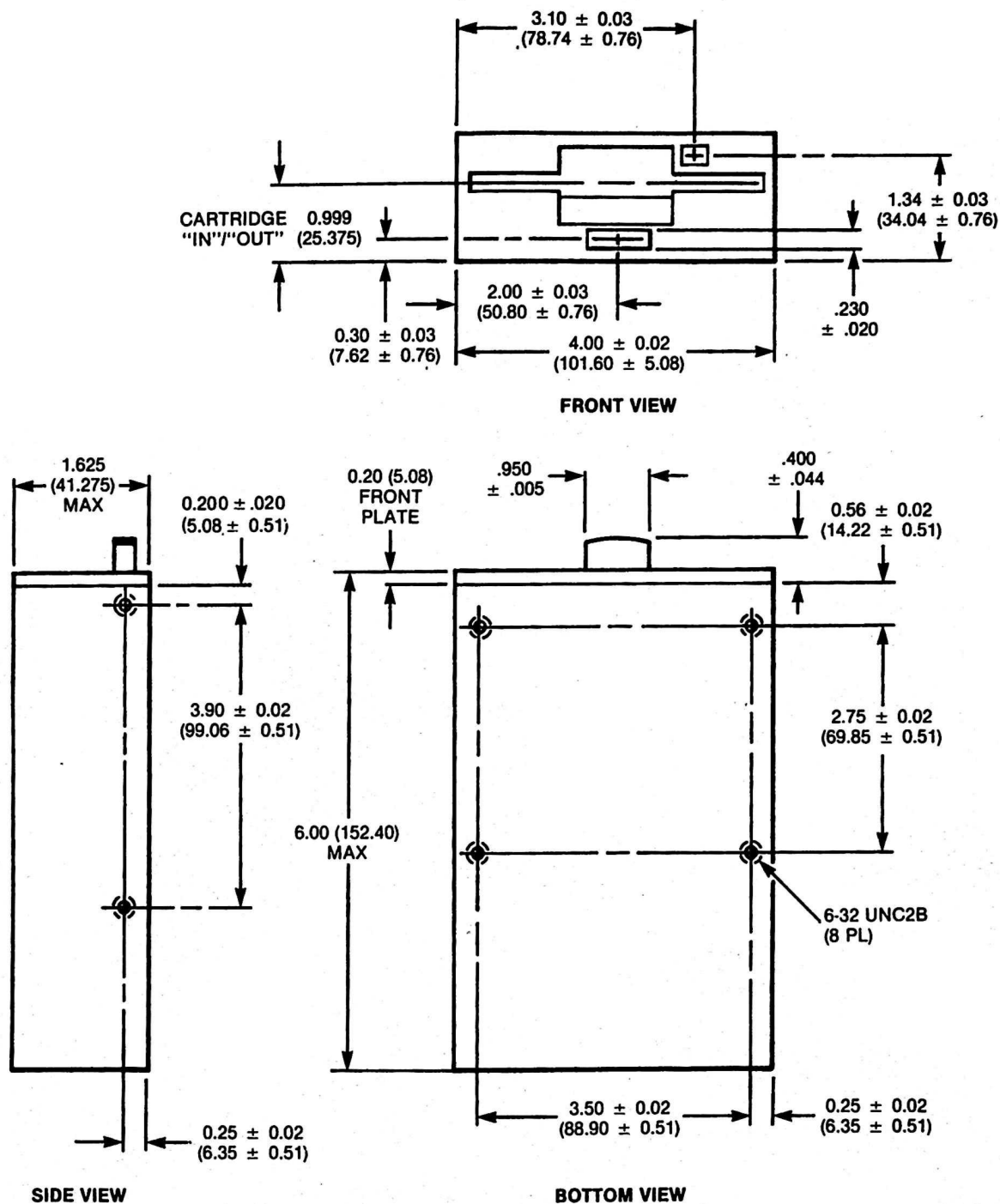


FIGURE 4-1. RECOMMENDED MOUNTING POSITIONS

39254-14

4.3 MECHANICAL DIMENSIONS

See figure 4-2 for dimensions of the SA300.



39254-15

FIGURE 4-2. SA300 PHYSICAL DIMENSIONS

SECTION VIII OPERATION PROCEDURES

8.1 INTRODUCTION

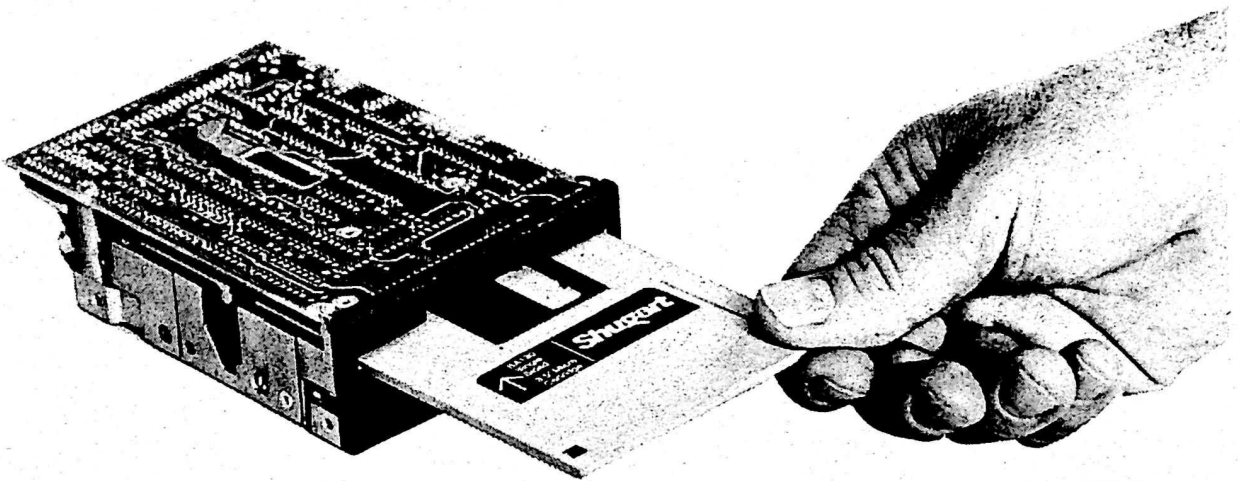
The SA300 was designed for ease of operator use to facilitate a wide range of operator oriented applications. The following paragraphs are a guide for the handling procedures on the microcartridge and microfloppy drive.

8.2 MICROCARTRIDGE LOADING

To load the microcartridge, insert the cartridge, auto shutter first, with the label facing up. Push in the cartridge. A mechanical interlock ensures proper media insertion. See figure 8-1 for insertion illustration. Figure 8-2 provides nomenclature description.

If the cartridge fails to load, press the eject button, then reinsert cartridge.

To remove the cartridge, push the eject button. The cartridge will automatically eject.



39254-19

FIGURE 8-1. MICROCARTRIDGE LOADING

8.3 MICROCARTRIDGE HANDLING

To protect the cartridge, the same care and handling procedures specified for computer magnetic tape apply. These precautionary procedures are as follows:

- a. Cartridges not intended for immediate use should be stored in the box.
- b. Keep cartridges away from magnetic fields and from ferromagnetic materials which might become magnetized. Strong magnetic fields can distort recorded data on disk.
- c. Place I.D. labels in correct location, never use in layers.
- d. Do not use erasers.
- e. Heat and contamination from carelessly dropped ash could damage disk.
- f. Do not expose cartridge to heat or sunlight.

MICRO CARTRIDGE TERMINOLOGY

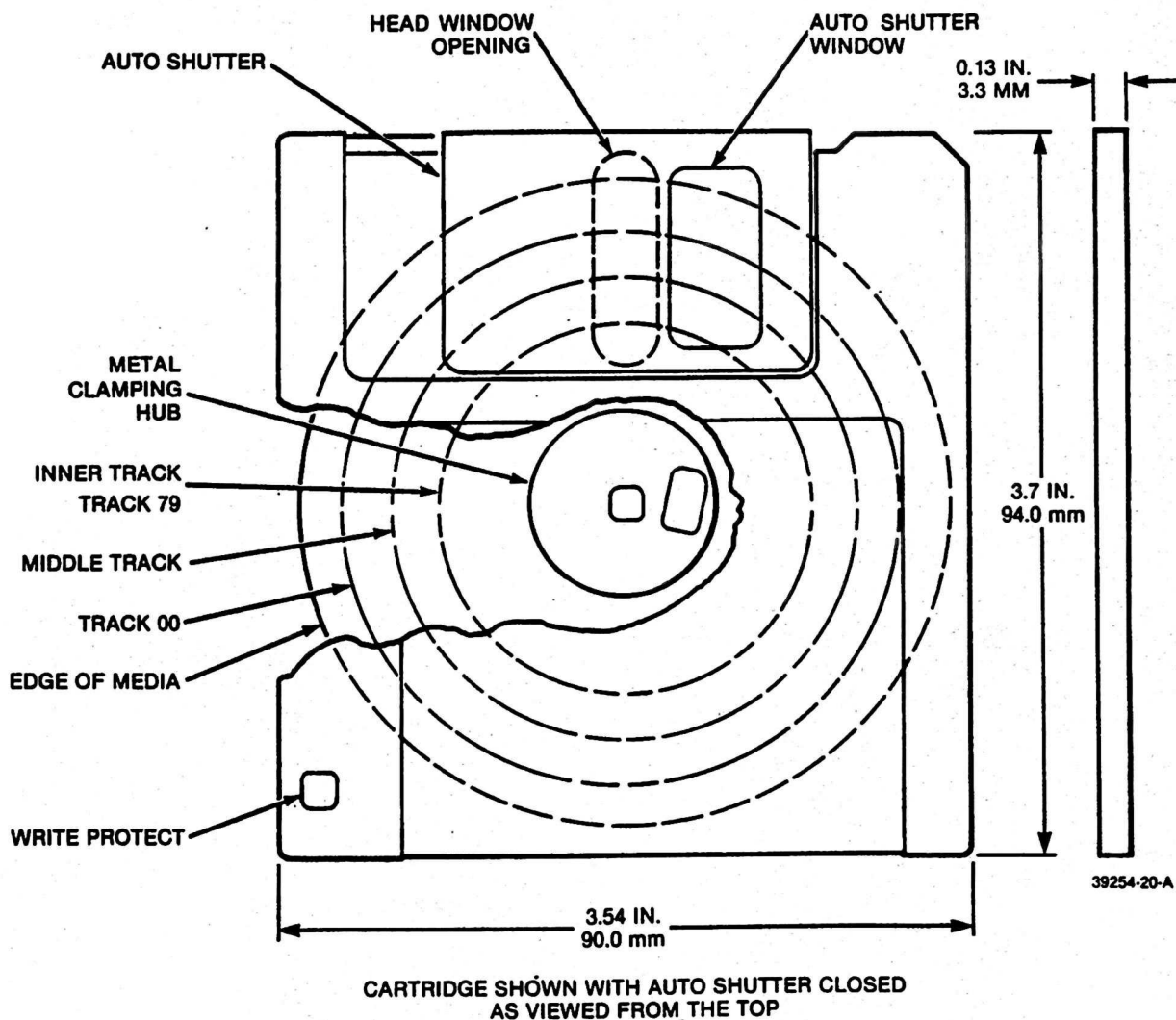


FIGURE 8-2. SA130 MICROCARTRIDGE NOMENCLATURE

8.4 WRITE PROTECT FEATURE

The microcartridge comes with a mechanical write protect tab. To write protect the cartridge, turn the mechanical tab as shown in figure 8-3 to uncover the write protect hole.

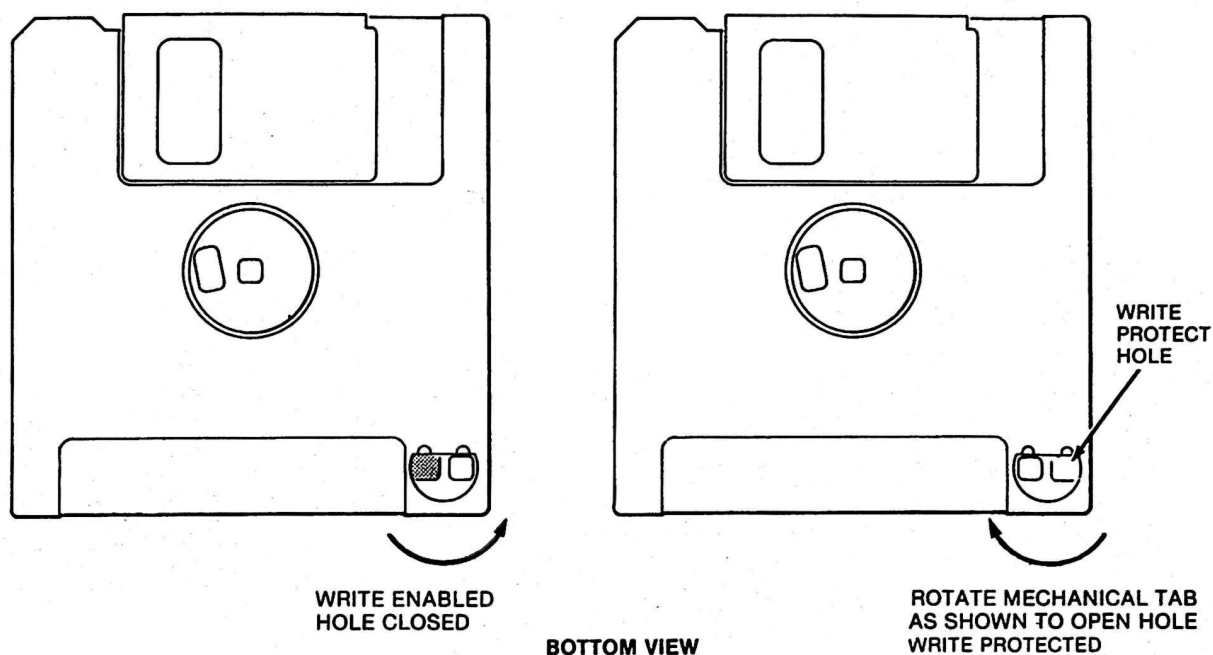


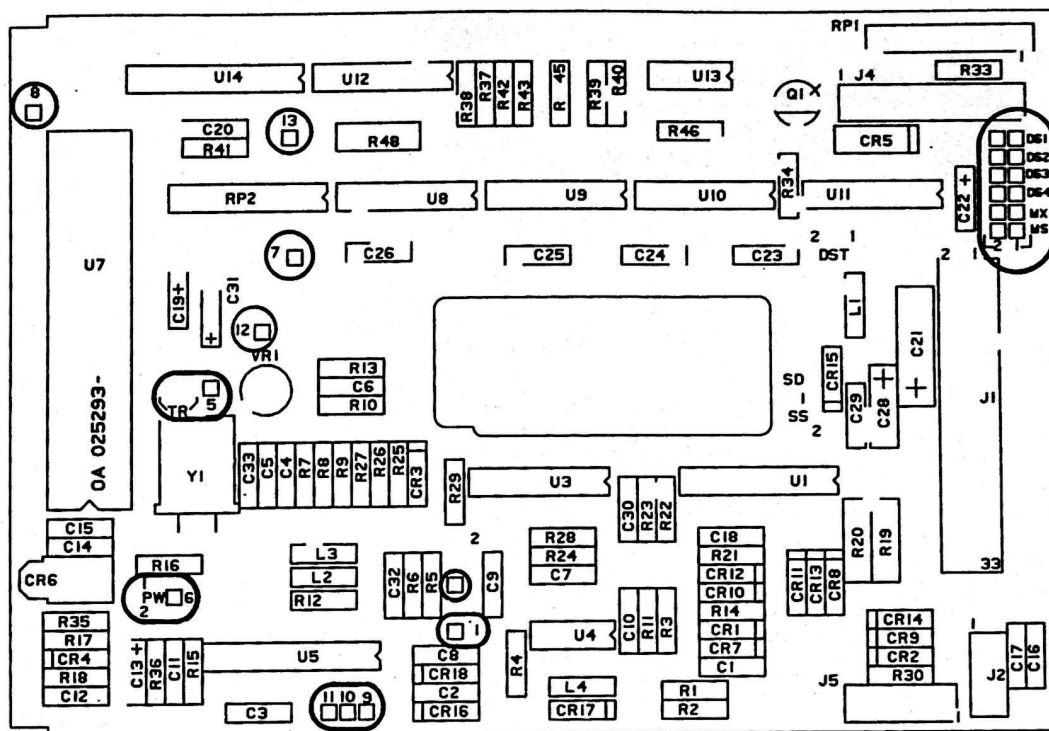
FIGURE 8-3. SA300 WRITE PROTECT OPERATION

39254-21

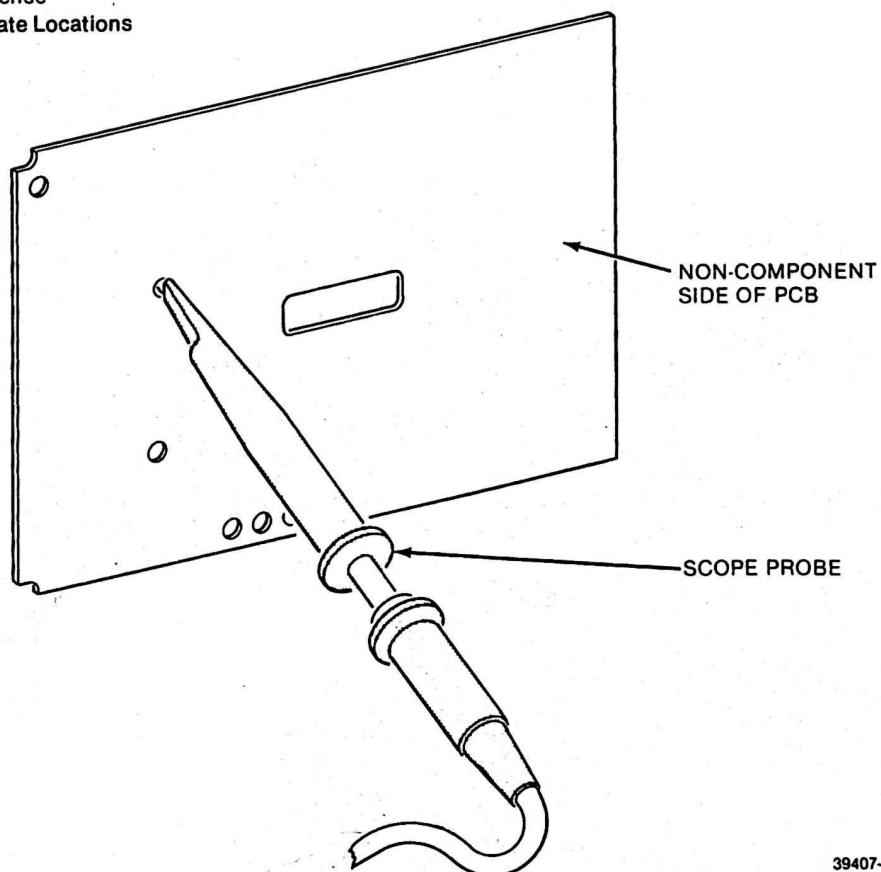
8.5 TEST POINT USAGE

The microfloppy PCB is mounted with the solder (non-component) side out. The test points required for drive testing can be accessed without removing the PCB. Holes are provided in the board which have traces connected to them on the component side. To reach the test point, insert and attach a hook-type scope probe to the side of the test point hole.

See figure 8-4 for test point locations and probe positioning.



TP1 and TP2 Analog Read Data
 TP0 Ground
 TP6 Digital Read Data
 TP7 + Index
 TP8 + Track 00 Sense
 Circled Areas Indicate Locations



39407-10

FIGURE 8-4. TEST POINT, JUMPER LOCATIONS AND PROBE POSITIONING